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THESIS

A DIGITAL RECORDING SYSTEM FOR SPACE-BASED APPLICATIONS UTILIZING FOUR-MEGABIT MAGNETIC BUBBLE MEMORIES

by

Bruce A. Campbell

June 1985

Thesis Advisor: R. Panholzer

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A modular combination of Intel Corp. state-of-the-art four-megabit magnetic bubble memory components is presented which can be configured as a digital data recorder of variable capacity and input rate.

A description of magnetic bubble memory technology and operation is included in an appendix.

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A Digital Recording System
for Space-Based Applications
Utilizing Four-Megabit Magnetic Bubble Memories

by

Bruce A. Campbell
Lieutenant, United States Navy
B.S. Aerospace Engineering, U.S. Naval Academy, 1977

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

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June 1985

ABSTRACT

Magnetic bubble memory technology offers several desirable characteristics for applications in space as a mass data recording and storage system.

A modular combination of Intel Corp. state-of-the-art four-megabit magnetic bubble memory components is presented which can be configured as a digital data recorder of variable capacity and input rate.

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TABLE OF CONTENTS

I. INTRODUCTION 13
  A. MAGNETIC BUBBLE MEMORIES AND SPACE APPLICATIONS 13

II. A MAGNETIC BUBBLE MEMORY SYSTEM 18
  A. THE FOUR-MEGABIT MAGNETIC BUBBLE MEMORY MODULE 19
    1. The 7114 Magnetic Bubble Memory Chip . . . 21
    2. The 7250 Coil Pre-Driver Chip and 7264 Coil Drive Transistors 23
    3. The 7234 Current Pulse Generator Chip . . 24
    4. The 7245 Formatter/Sense Amplifier Chip 25
    5. The Four-Megabit Memory "Module" 27
  B. THE 7225 BUBBLE MEMORY CONTROLLER 27
    1. Bubble Memory Signals 29
    2. External System Interface 29
    3. Parallel Controller Capability 30
    4. Internal Operations 30
    5. A Four-Megabit Magnetic Bubble Memory System 32
  C. MULTIPLE MEMORY MODULE SYSTEMS 32
    1. Multi-Module Interfacing 32
    2. Multi-Module Operations 33
  D. THE EIGHT-MODULE MAGNETIC BUBBLE MEMORY BOARD 37
    1. Memory Capacity 37
    2. Data Rates 38
    3. Transfer Page Size 38

4. Power Consumption 38
5. Size/Weight 39
E. PARALLEL CONTROLLER OPERATION 42

III. MAGNETIC BUBBLE MEMORY SYSTEM OPERATION 44
A. BMC - EXTERNAL SYSTEM COMMUNICATIONS 45
1. Command/Status Port 46
2. Register Address Counter 46
3. Parametric Registers 48
4. FIFO 53
5. Error Correction 53
6. BMC Status Register 56
7. Commands 57
B. NORMAL OPERATING PROCEDURES 59
1. Power-Up and Command Execution 59
2. Power Down 62

IV. A MAGNETIC BUBBLE MEMORY DIGITAL RECORDER 64
A. SYSTEM DESIGN LOGIC 64
1. Memory Capacity 64
2. Data Rate 64
B. N.P.S. PROTOTYPE DIGITAL RECORDER 66
1. Background 66
2. Experiment Description 66
3. Recorder Requirements 67
4. BPK 5V75A Prototype Kit Design 67
5. Multi-Module Custom Design 68

APPENDIX A: MAGNETIC BUBBLE MEMORY TECHNOLOGY 71
A. MAGNETIC BUBBLE MEMORY CELL DESCRIPTION . . . 71
1. Substrate 71
2. Permanent Magnet 72
3. Location and Movement of Data Bubbles . . 73
4. Data Storage Organization 79
5. Data Bubble Production 81

6. Data Input 83
7. Data Output 84
8. Bubble Detection 84
9. Data Organization and Addressing 85
10. Memory Cell Components 86
B. MEMORY CELL REQUIRED SUPPORT 87
1. Current Pulse Production 88
2. Input/Output Formatter 89
3. Controller 89

APPENDIX B: INTEL CORP. MAGNETIC BUBBLE MEMORY COMPONENTS 90
A. THE 7114 MAGNETIC BUBBLE MEMORY CHIP 91
1. Data Storage Configuration 92
2. Data Input/Output 94
3. Bootloop 95
B. THE INTEL 7250 COIL PRE-DRIVER CHIP AND 7264 COIL DRIVE TRANSISTORS 96
1. 7250 Coil Pre-Driver 96
2. 7264 Coil Drive Transistors 97
C. THE INTEL 7234 CURRENT PULSE GENERATOR CHIP 97
D. THE INTEL 7244 FORMATTER/SENSE AMPLIFIER CHIP 98
E. THE FOUR-MEGABIT MEMORY MODULE 103
F. THE 7224 CONTROLLER 104
1. 7224 BMC Internal Configuration 105
G. MULTIPLE MODULE SYSTEM CONFIGURATIONS . . . 110
1. BMC - FSA Communications 110
H. OPERATING LIMITATIONS AND REQUIREMENTS . . . 116
1. Operating Limitations 116
2. Voltage Regulator Circuitry 116
3. Powerfail Circuit 117
I. THE BPK 5V75A PROTOTYPE KIT 118

LIST OF REFERENCES 120

BIBLIOGRAPHY 122

INITIAL DISTRIBUTION LIST 123

LIST OF TABLES

1. Bubble Memory Comparison 15
2. Serial Memory System Operating Parameters 36
3. Eight-Module Memory Board Performance 39
4. Eight-Module Memory Board Power Requirements . . . 40
5. Command/Status Port Functions 46
6. Register Address Counter Assignments 47
7. Memory Module Addressing Scheme 51
8. Error Correction Levels 55
9. BMC Command Set 58
10. 7114 MBM Pin-Out Signal Descriptions 93
11. 7250 CPD Pin-Cut Signal Descriptions 97
12. 7264 CDT Pin-Out Signal Descriptions 99
13. 7234 CPG Pin-Out Signal Descriptions 100
14. 7244 FSA Pin-Out Signal Descriptions 102
15. FSA Command Codes 104
16. 7224 BMC Pin-Cut Signal Descriptions 106
17. 7224 BMC Pin-Cut Signal Descriptions (cont.) . . 108
18. 7114 Absolute Maximum Ratings 117

LIST OF FIGURES

1.1 Memory Technology Comparison 14
1.2 Cost per Bit vs. Access Time 16
1.3 Memory Capacity vs. Access Time 17
2.1 Bubble Memory System Components 20
2.2 7114 Magnetic Bubble Memory Chip Assembly 21
2.3 7114 Magnetic Bubble Memory Chip Signals 23
2.4 7250 CPD and 7264 CDT Signals 24
2.5 7234 Current Pulse Generator Chip Signals 25
2.6 7245 Formatter/Sense Amp Chip Signals 26
2.7 7225 Bubble Memory Controller Signals 28
2.8 Four-Megabit Magnetic Bubble Memory System 33
2.9 Multiple Memory Module System Configuration 34
2.10 Memory Module Approximate Area 41
2.11 Eight-Module Memory Board 42
3.1 7225 BMC - External System Interface 45
3.2 Block Length Register 49
3.3 Address Register 50
3.4 Enable Register 52
3.5 7224 Status Register 56
3.6 Memory System Power-Up Sequence 60
3.7 Memory System Initialization 61
3.8 Memory System Command Execution 62
3.9 Data Transfer Procedure 63
A.1 Magnetic Substrate and Effects of an Applied Perpendicular Magnetic Field 72
A.2 Wide-Gap Permalloy Structure Designs 73
A.3 Magnified View of Chevrons on Substrate 74
A.4 Orientation of the Substrate and Magnets 75

A.5 Rotating Magnetic Field Circuit and Waveforms . . . 77
A.6 Movement of Bubbles Beneath a Permalloy Structure Due to a Rotating Magnetic Field 78
A.7 Single Loop Bubble Storage Architecture 79
A.8 Major/Minor Loop Bubble Storage Architecture . . . 80
A.9 Bubble Generation for Input 82
A.10 Input of Data to a Storage Loop 84
A.11 Output of Data from a Storage Loop 85
A.12 Magnetic Bubble Detection Circuit 86
A.13 An Exploded View of a Memory Cell 87
A.14 Magnetic Bubble Memory Required Systems 88
B.1 7114 Magnetic Bubble Memory Chip Schematic 92
B.2 Intel 7114 Bubble Memory Chip Data Organization . . 94
B.3 7250 Coil Pre-Driver Chip Schematic 96
B.4 7264 Coil Drive Transistor Schematic 98
B.5 7234 Current Pulse Generator Chip Schematic 99
B.6 7244 Formatter/Sense Amp Chip Schematic 101
B.7 7244 Formatter/Sense Amp Internal Block Diagram . 103
B.8 7224 Bubble Memory Controller Chip Schematic . . 105
B.9 7224 BMC Internal Configuration Block Diagram . . 109
B.10 Four-Megabit System Circuit Diagram 111
B.11 Memory System Expansion 112
B.12 BMC - FSA Communications 113
B.13 Access and Command of Multiple Memory Modules . . 114
B.14 Multiple Module Data Transfers 116
B.15 Voltage Regulator Circuit 118
B.16 BPK 5V75A Prototype Kit 119

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"My head I'd be scratchin'
while my thoughts were busy hatchin'
if I only had a brain."

I. INTRODUCTION

A. MAGNETIC BUBBLE MEMORIES AND SPACE APPLICATIONS

[Ref. 1] states that the desired characteristics for space-based memory systems are non-volatility, versatility, reliability and ruggedness, and cost effectiveness. [Ref. 2] is more specific in stressing the importance of radiation hardness and constraints on physical size, weight, and power consumption of all space-based systems.

Many of the references surveyed for this paper describe benefits offered by magnetic bubble memory systems for applications in space. Most of these benefits are attributable to the physical properties of magnetic bubble memories.

The cost for placing a specific payload into space is derived from both the weight and the volume of the system. Magnetic bubble memories are light-weight, compact, solid-state digital data storage systems configureable in many ways to fit different requirements in size and weight, as well as performance.

Space is a harsh environment for which the solid-state nature of magnetic bubble memory is well suited. Some memories, such as analog tape recording systems and disk/drum units, have moving parts which may need lubricants, an atmosphere, and a controlled environment for proper operation. Solid-state magnetic bubble memories have no moving parts, are operable in the vacuum of space, and over a wide range of temperatures. The relatively rugged solid-state construction also allows easier design in withstanding the shocks and vibrations experienced by space systems during launch and maneuvers.

Ambient radiation and its effect on stored digital information is another problem still under investigation [Ref. 3]. While its associated support components are ordinary solid-state elements routinely used in space today, the data-storing magnetic bubble memory chip is surrounded by permanent magnets, field-producing coils, and a shield to isolate these strong magnetic fields from nearby systems. This configuration makes magnetic bubble memory chips naturally harder to radiation effects than ordinary solid state memory components.

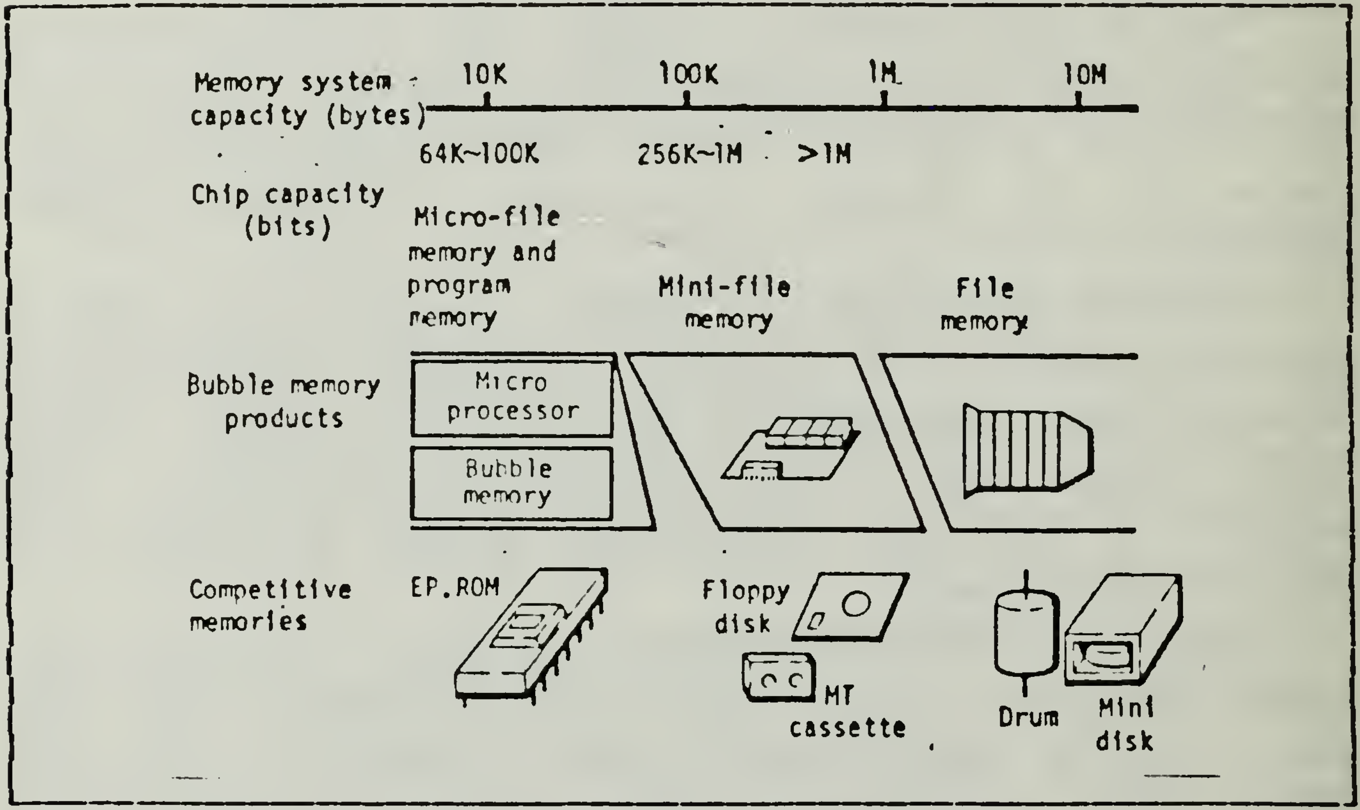

Figure 1.1 Memory Technology Comparison.

Power consumption is another major concern of space system engineers. A magnetic bubble memory consumes power only when data is being transferred or when the system is being prepared for transfers. No power is required to maintain data within a magnetic bubble memory system, unlike systems using other solid-state storage technologies such as charged couple devices or random access memories. This characteristic is especially attractive for space systems which store recorded data for later transmission to a ground station [Ref. 4] or for systems which must be capable of retaining alterable instructions indefinitely for later implementation at a deep-space destination [Ref. 5].

TABLE 1

Bubble Memory Comparison

ADVANTAGES		DISADVANTAGES
Higher reliability Non-mechanical Smaller size Faster access Simpler interface Media integrity	Bubble memory vs Floppy disk	Stored data not readily changed
Non-volatile More bits per device Reduced board space	Bubble memory vs RAM	Slower access Slower transfer rate
Programmability More bits per device Less board space	Bubble memory vs ROM or PROM	Slower access Slower transfer rate

Magnetic bubble memory systems have inherently slow access times due to the physical arrangement of the data storage architecture. This limits their usefulness in high-speed data storage and retrieval, such as required in a main-frame type computing system. However, magnetic bubble memory systems provide an excellent means for mass data recording and storage. The modular characteristics of present magnetic bubble memory designs permit custom configuration to meet virtually any recording need in terms of data input rates and memory capacities by varied combinations of discrete memory units.

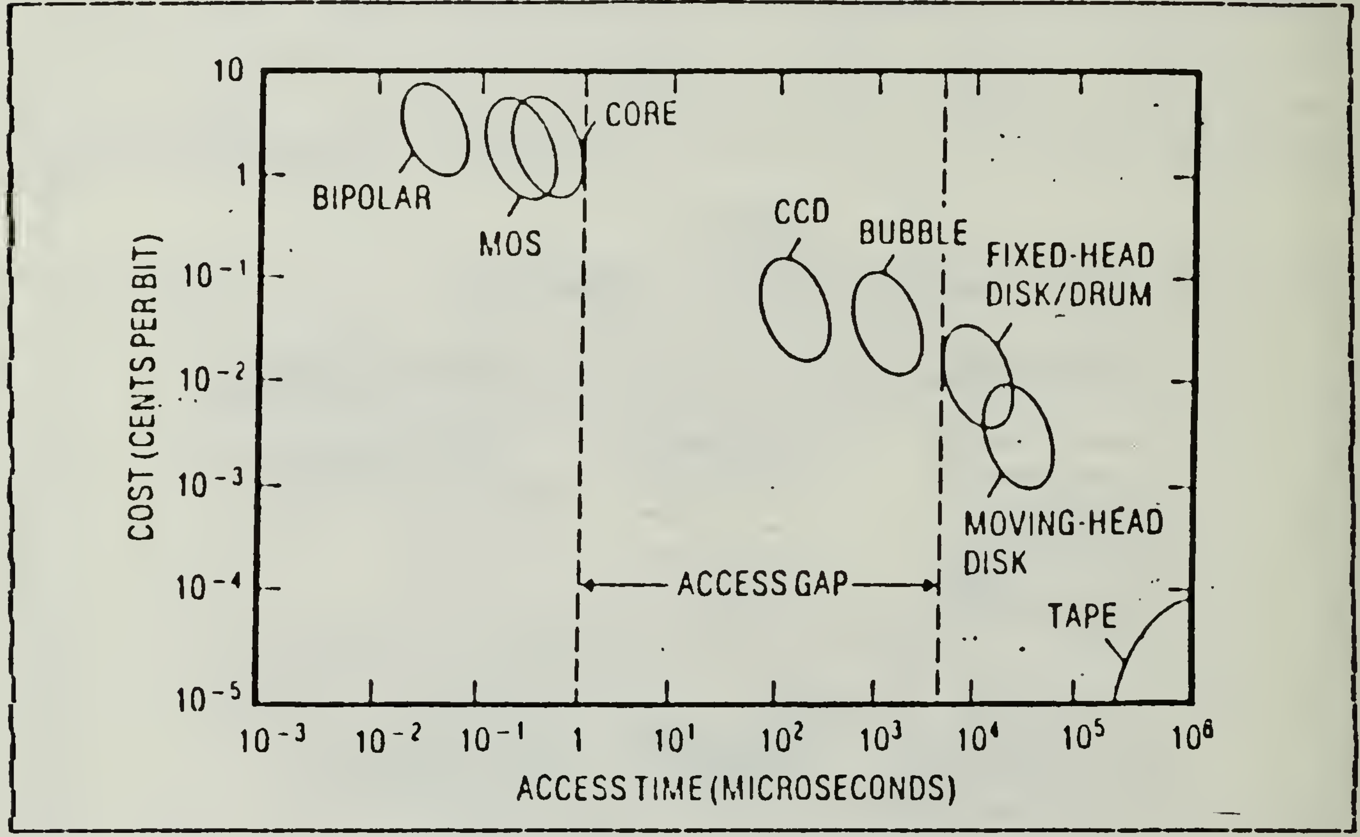

Figure 1.2 Cost per Bit vs. Access Time.

Figure 1.1 illustrates the memory capacities associated with different types of memory uses and indicates the competitive memory systems within each type. The figure suggests that, due to the modularity of this type of system, magnetic bubble memories could be configured for use in all these types of memory applications.

Table 1 lists bubble memory advantages and disadvantages when compared with some competitive memory systems.

The following figures compare magnetic bubble memory technology with other memory technologies using access time

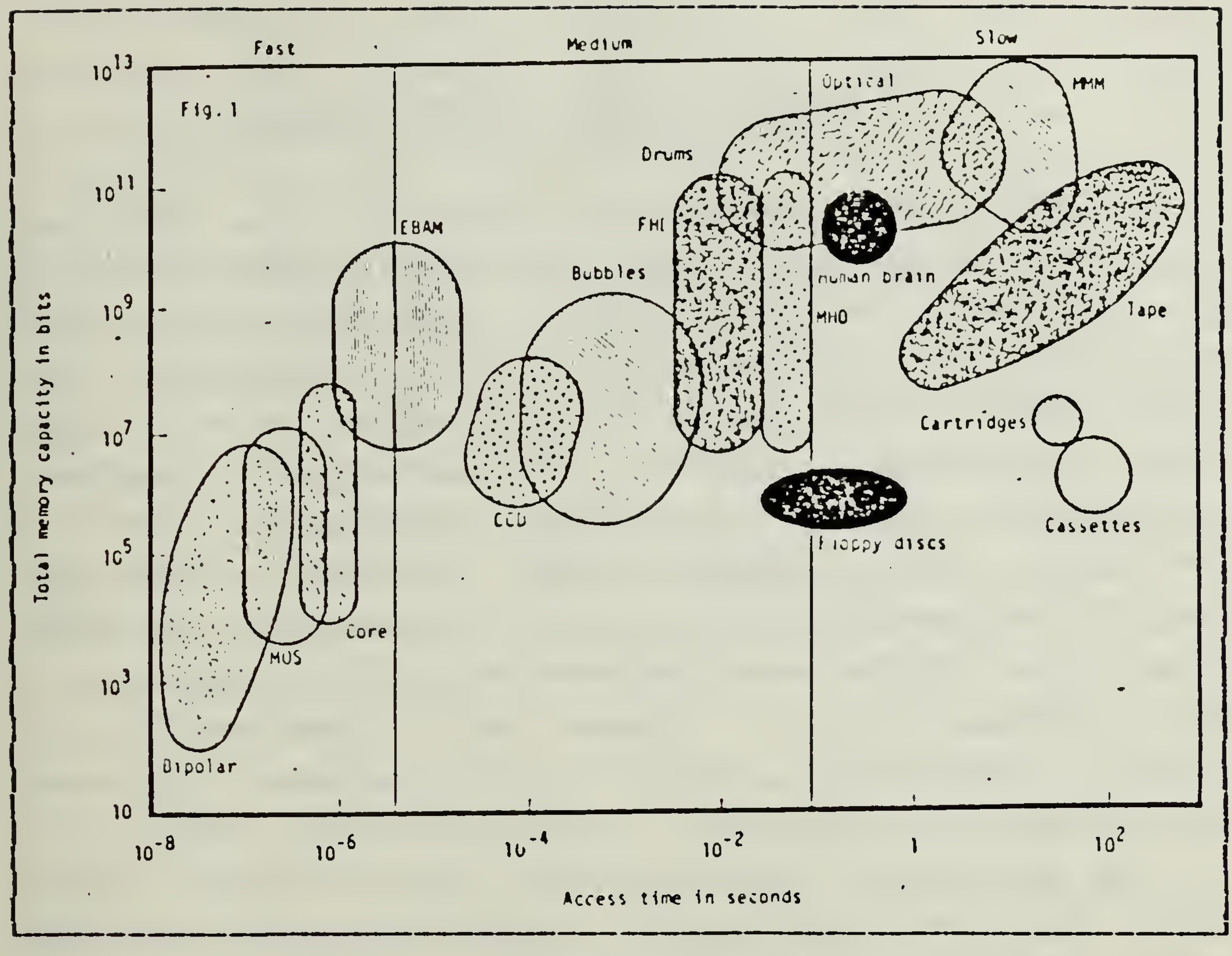

Figure 1.3 Memory Capacity vs. Access Time.

as a common denominator. Figure 1.2 [Ref. 6] indicates magnetic bubble memory comparative cost and figure 1.3 [Ref. 7] compares the expected performance of magnetic bubble memories with other memory systems. In both comparisons it is seen that magnetic bubble memories fill a gap, in terms of these performance measures, when compared to all technologies in general use. However, not all these technologies are as suitable for space-based applications and none offer as many benefits for such use as does magnetic bubble memory.

II. A MAGNETIC BUBBLE MEMORY SYSTEM

In 1979 Intel Corporation of Santa Clara, Ca. introduced a digital data storage and retrieval system based on magnetic bubble technology [Ref. 8]. The system was capable of storing up to one-megabit of digital information in a single bubble memory chip with the aid of a family of components performing support and interface functions. Improvements, mainly in production techniques, allowed an increase in storage capacity within the same storage area [Ref. 9] and resulted in the recent release of a new family of magnetic bubble memory components with a single bubble memory chip capable of storing up to four-megabits of digital information. This is the maximum single-chip storage capability available in this technology today.

The advantage offered by the Intel magnetic bubble memory chip family is the ease with which a magnetic bubble memory system can be implemented. The elements of the system can be combined to form modular components which may be configured in many ways to provide different capabilities in terms of data rate and storage capacity.

Early designs required the user to be concerned with overseeing proper operation of the magnetic bubble system internal functions as well as control of data flow into and out of the memory [Ref. 10]. Intel components feature a dedicated bubble memory controller to perform these internal functions independently and serve as a simple interface between the memory and the external system.

This chapter introduces the Intel components which can be used to design a magnetic bubble memory system. The first section describes the individual components which make up a magnetic bubble memory "module" capable of storing four-megabits of digital information. The second section describes the controller chip which coordinates memory access functions within a module. Configurations associating multiple memory "modules" with a single bubble memory controller are discussed in the third section. A four-megabyte configuration, incorporating eight memory modules and one bubble memory controller on a single board, is described in the fourth section. This represents the basic element used in the proposed design of a digital data recorder for space-based applications presented in Chapter 4. The last section describes the capability for parallel controller operations which enhances even further the possible performance of the magnetic bubble memory system.

Appendix A presents an explanation of the basic operation of a magnetic bubble memory. It is assumed that the reader is familiar with this information and only a functional description of the role each component performs in magnetic bubble memory system operation is presented in this chapter. Appendix B contains a more detailed description of the available Intel magnetic bubble memory components.

Readers should be particularly aware that this chapter and the following proposed designs incorporate the expected capabilities of the 7225 bubble memory controller and 7245 formatter/sense amplifier chips not yet available as production components. This is explained more fully in the introduction to Appendix E.

A. THE FOUR-MEGABIT MAGNETIC BUBBLE MEMORY MODULE

Figure 2.1 depicts the Intel Corp. components used to construct a magnetic bubble memory system capable of storing four-megabits of digital information.

The components listed below the 7225 BMC combine to form a memory "module" which represents the basic block of

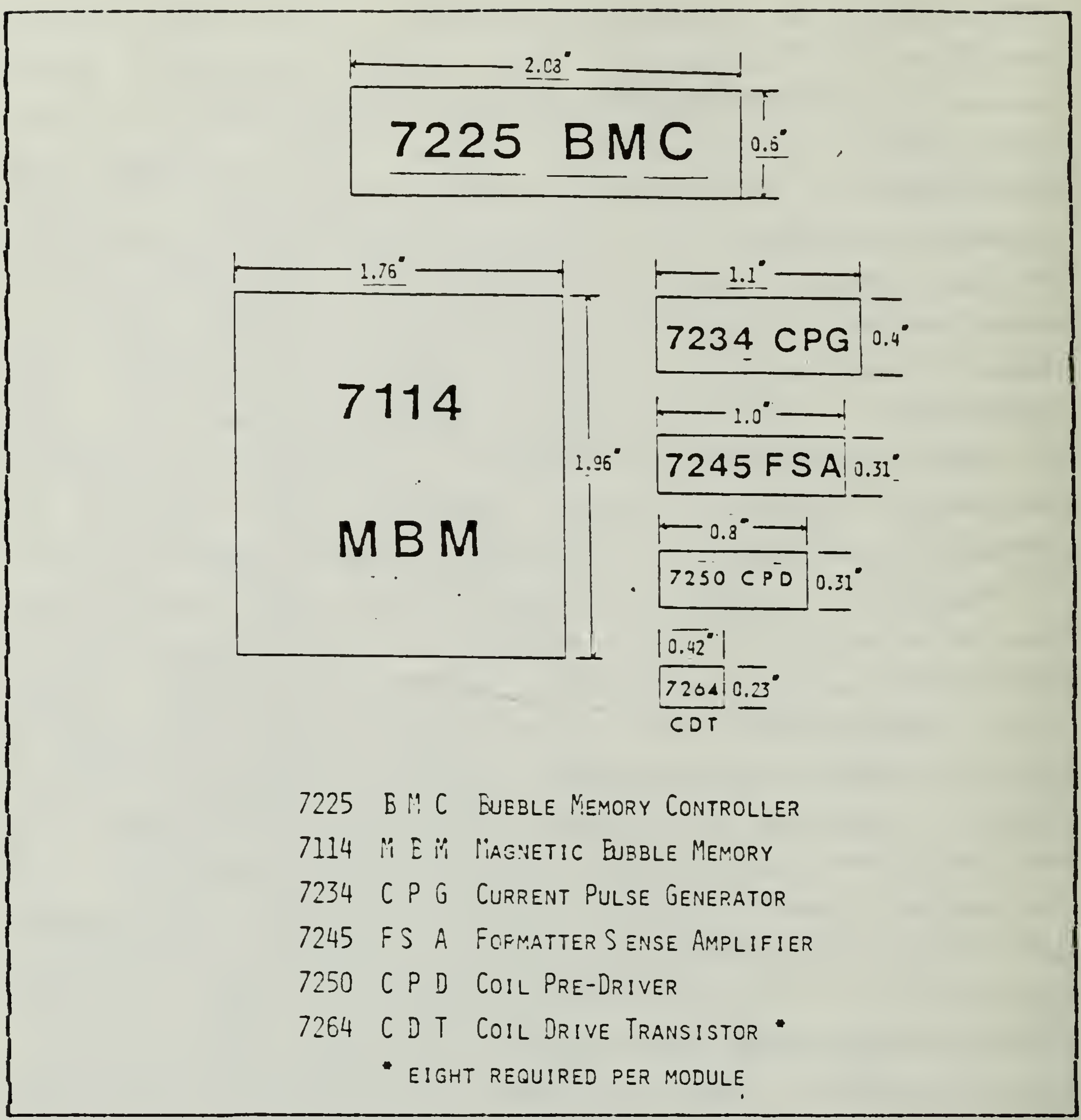
2.03"
7225 BMC
0.6"
1.76"
7114
MBM
1.96"
1.1"
7234 CPG
0.4"
1.0"
7245 FSA
0.31"
0.8"
7250 CPD
0.31"
0.42"
7264
0.23"
CDT
7225 B M C Bubble Memory Controller
7114 M B M Magnetic Bubble Memory
7234 C P G Current Pulse Generator
7245 F S A Formatter Sense Amplifier
7250 C P D Coil Pre-Driver
7264 C D T Coil Drive Transistor *
* Eight required per module

Figure 2.1 Bubble Memory System Components.

storage capacity on which designs of systems with higher capacities and capabilities are based. The module contains a single bubble memory chip and support components which must accompany each memory chip for proper operation.

Since the bubble memory controller may be associated with multiple memory modules, description of this component is provided separately in the next section.

1. The 7114 Magnetic Bubble Memory Chip

The 7114 magnetic bubble memory (MBM) chip contains the substrate in which magnetic bubbles are stored, the permalloy structures which determine bubble location, the permanent magnets which ensure bubble stability, and the perpendicular coils which control bubble movement. The entire assembly is enclosed in a case designed to protect internal and external components from stray magnetic fields (Figure 2.2).

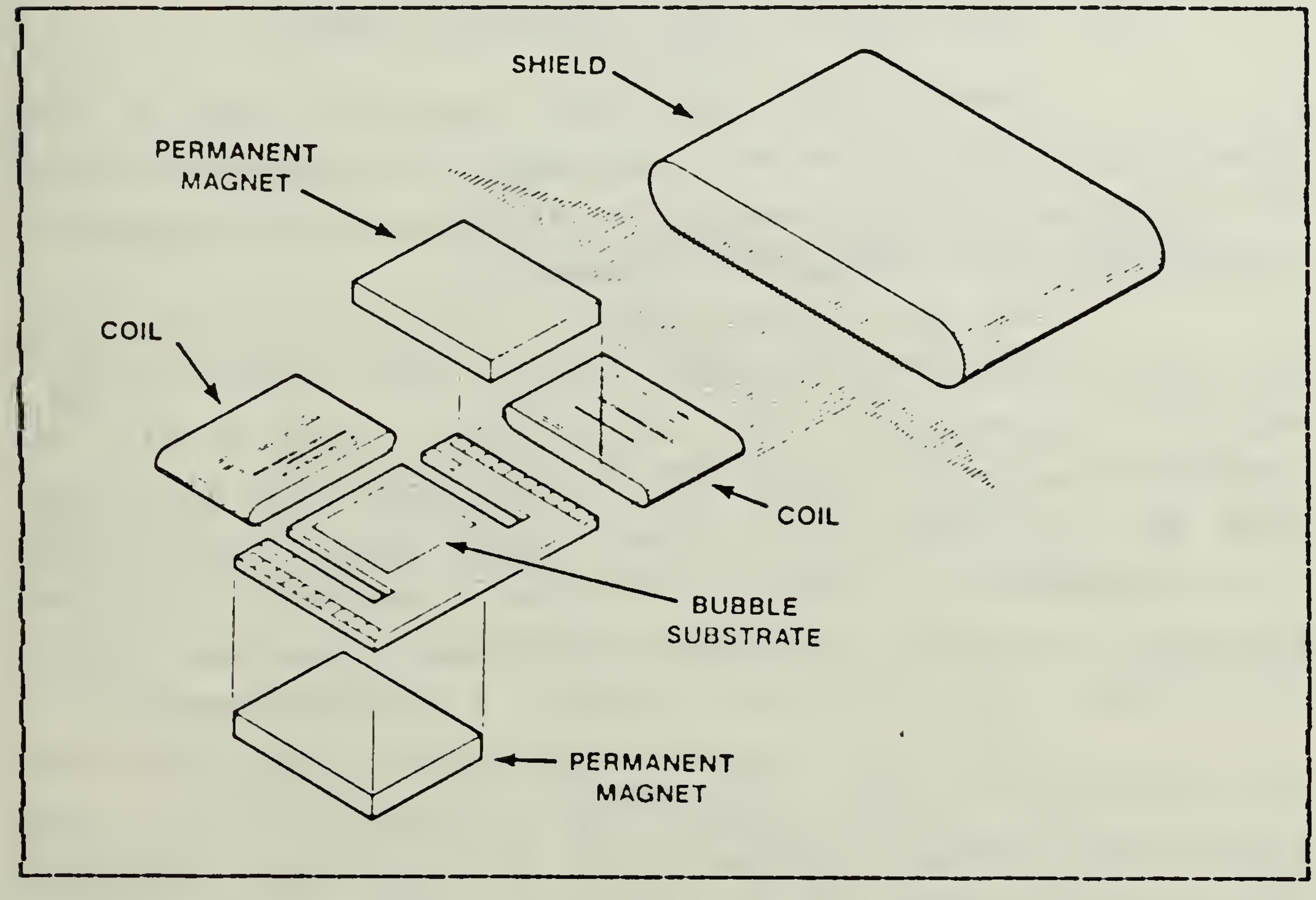

Figure 2.2 7114 Magnetic Bubble Memory Chip Assembly.

a. Data Organization

The major-track/minor-loop data storage architecture of the 7114 MBM consists of 512 storage "loops" with 8192 discrete locations per loop providing a maximum user storage capability of 4,194,304 bits (four-megabits) of digital information. This architecture requires transfer of data in "pages" of 512 bits (64 bytes) of information each input/output operation, corresponding to one bit of information per storage loop. Each chip can store up to 8192 data pages.

b. Bootloop and Error Correction Codes

Twenty-eight additional loops are used to store twenty-eight bits of error correcting code appended to each data page input to the memory for storage. Error correcting capabilities are discussed in Chapter 3.

Two more loops contain the bootloop information specific for each bubble memory chip. These loops contain a digital representation of the operating loops within the chip and a synchronization code which identifies the reference page from which all other stored pages are located. This information is used by the support components to format the data correctly for input and output operations and to keep track of data flow and placement within the memory.

Figure 2.3 depicts the signals associated with the 7114 MBM. These signals are provided by or to the support chips under guidance of the bubble memory controller to perform the functions necessary for proper memory operation as described in Appendix A, namely: establishment of a rotating magnetic field for bubble movement within the memory, signals to generate data bubbles from seed bubbles for input, swap and replicate signals for bubble movement into and out of the storage loops, and detection of voltage

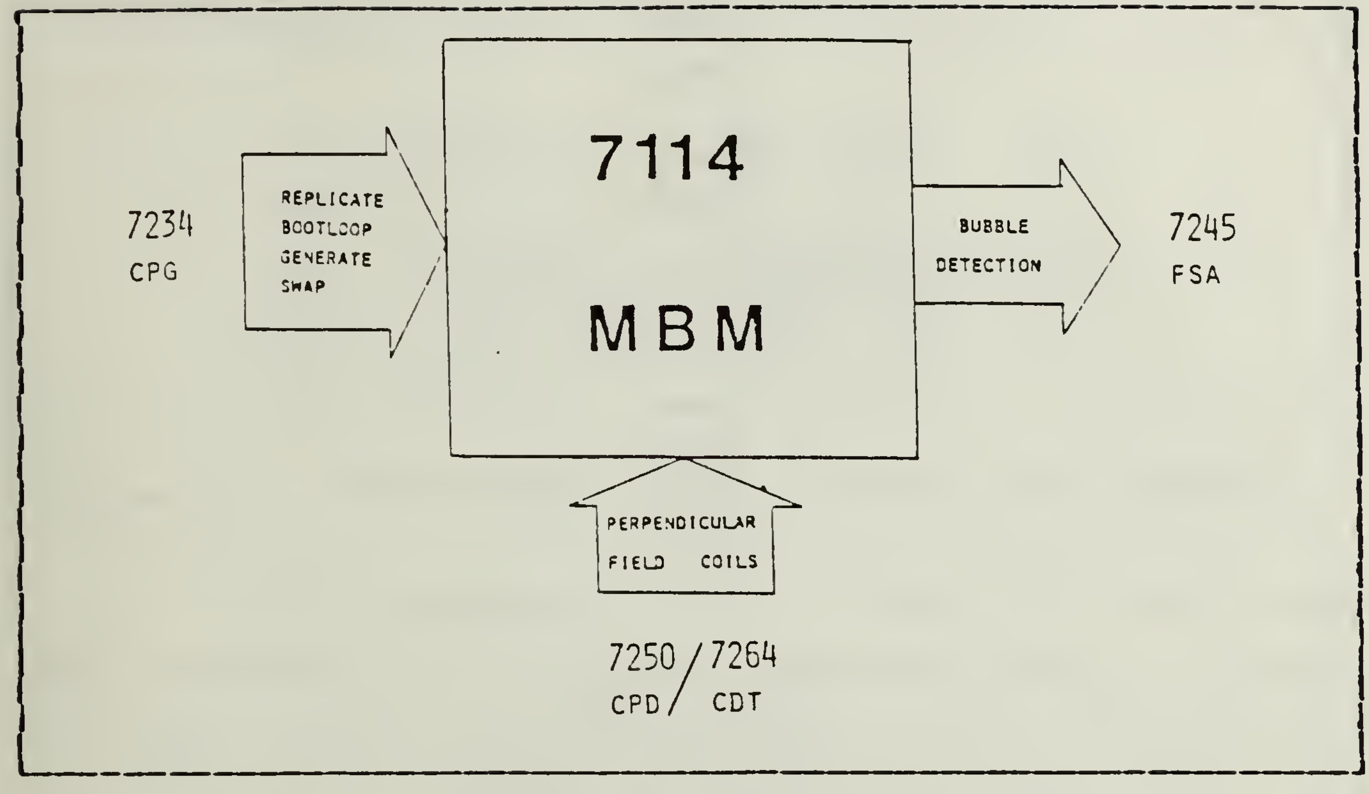

Figure 2.3 7114 Magnetic Bubble Memory Chip Signals.

signals from the detector circuits for data output from the memory.

The following subsections describe the support components that perform most of these functions and which must accompany each memory chip for proper operation.

2. The 7250 Coil Pre-Driver Chip and 7264 Coil Drive Transistors

Figure 2.4 depicts the 7250 coil pre-driver (CPD) chip and the two sets of four matched 7264 coil drive transistors (CDTs) used to produce current signals sent to the two perpendicular coils surrounding the substrate material within the 7114 MBM.

The 7250 CPD and 7264 CDTs produce triangular current waveforms which are applied in quadrature to the perpendicular coils based on timing signals from the bubble memory controller. This establishes a rotating magnetic

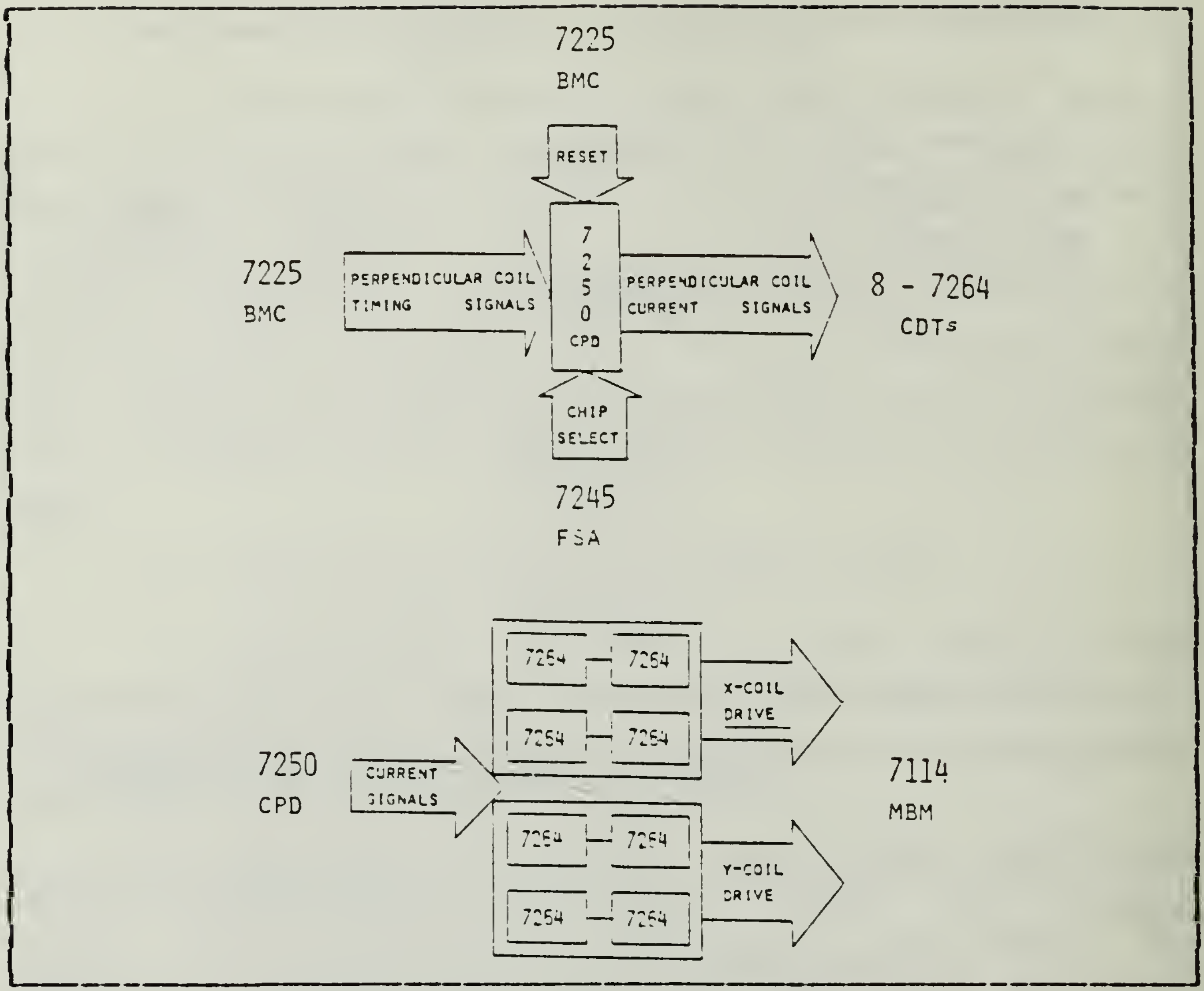

Figure 2.4   7250 CPD and 7264 CDT Signals.

field about the substrate which induces movement of stored magnetic bubbles within the 7114 MBM chip.

3. The 7234 Current Pulse Generator Chip

Figure 2.5 shows the signals associated with the 7234 current pulse generator (CPG) chip. Based on signals from both the bubble memory controller and the formatter/ sense amplifier chip, the 7234 CPG sends current pulse signals to the 7114 MBM which perform the generate, swap, and replicate functions necessary during read and write operations with the memory.

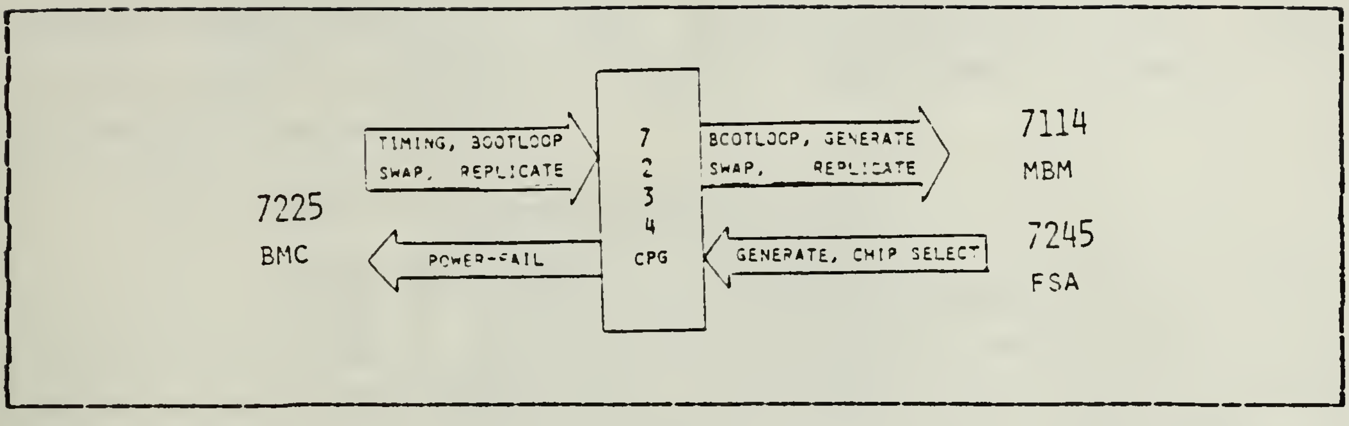

Figure 2.5 7234 Current Pulse Generator Chip Signals.

The 7234 receives both the 5-volt and 12-volt power supplies required by the memory system and acts as a monitor for these supplies. If either source falls below specified thresholds (Appendix B), a power-fail signal is sent to the bubble memory controller to aid in deactivation of the system in an orderly sequence to preserve data integrity.

4. The 7245 Formatter/Sense Amplifier Chip

The 7245[1] formatter/sense amplifier (FSA) interacts with each of the memory components and performs a number of functions concerned with data transfer within the system. Figure 2.6 depicts the numerous signals associated with the FSA and the other components involved.

a. External Signals

The bubble memory controller communicates with a memory module through the 7245 FSA via a single bi-directional serial data line (DIO). The level of the command/data (C/D) line specifies whether signals on the DIO are to be interpreted as commands or data. Direction of

---

[1] This section is based on information about the existing 7244 FSA chip and the expected capabilities of the 7245 chip as described in advance information provided by Intel. See Appendix B.

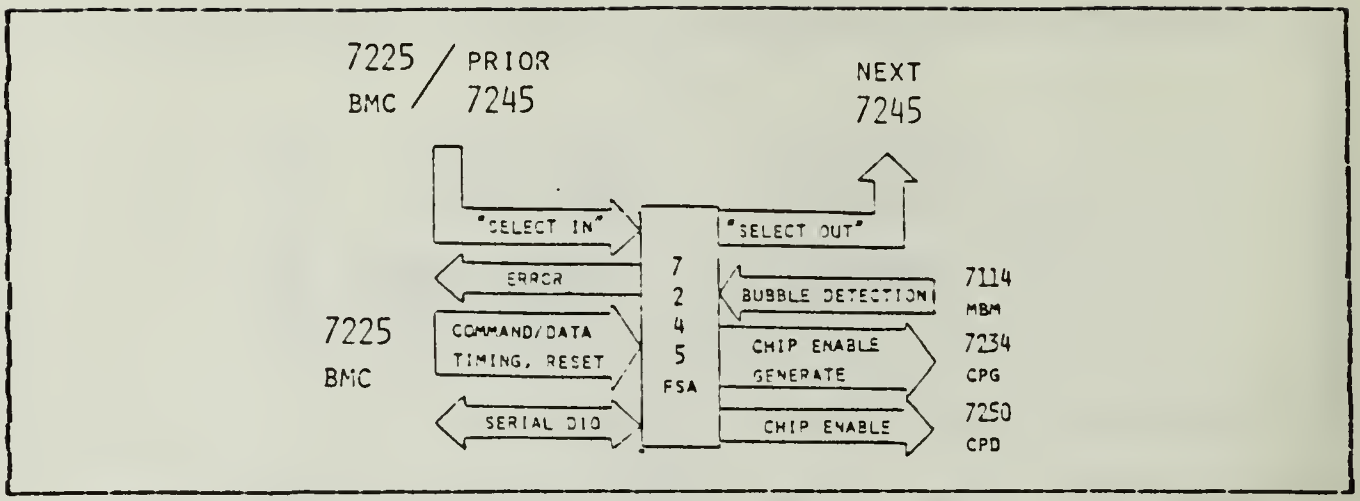

Figure 2.6 7245 Formatter/Sense Amp Chip Signals.

data flow on the DIO depends on the received command which dictates the memory operation to be performed. The controller also provides reset and timing signals and responds to error signals generated if a 7245 FSA built-in error correction scheme discovers a discrepancy during data extraction from the memory chip.

The bubble memory controller enables operation of a module and establishes communication with the FSA using the chip "select in" line. In multi-module configurations, this chip select signal is passed from module to module to establish a time-multiplexed communication between the bubble memory controller and each module FSA individually. This process is discussed again later in this chapter and explained in detail in Appendix B.

Bubble generate signals are sent to the 7234 CPG in proper sequence for data input to the memory. Millivolt signals from the bubble detection circuits are sensed and amplified during a memory read and reconstructed into the original data stream for output.

The 7245 also produces enable signals to the 7234 CPG and 7250 CPD chips. These components and the current supply to the 7114 MBM detection circuits are only enabled when required by the memory access operation. This reduces power consumption during times the system is not actively transferring data.

b. Internal Operations

The 7245 FSA is prepared for up-coming operations by the input of a four-bit command code sent by the bubble memory controller over the serial data line, with the appropriate level on the command/data line. The commands include initialize, reset, and memory read and write operations as well as specifying the error-correction scheme and checking of the FSA status register.

Data are passed through a 540-bit first-in/first-out (FIFO) buffer where 28 bits of error correcting code are appended or checked for each entire 512-bit page of data transferred.

Another register holds the bootloop information, extracted from the memory chip, used to correlate data with operating storage loops during input and output operations.

5. The Four-Megabit Memory "Module"

The components described above can be combined to form the basic block of memory storage capability which will be referred to as a memory "module". Each module is capable of transferring and storing up to four-megabits of digital information under guidance of a bubble memory controller. The controller, which may be associated with multiple memory modules, is described in the next section.

B. THE 7225 BUBBLE MEMORY CONTROLLER

Use of a dedicated device to control the internal functions required within the magnetic bubble memory system is an improvement over early designs in which the user was required to incorporate these functions into the overall operation of the system utilizing bubble memory. Intel components allow the designer to access the memory in much the same way as conventional memory systems, leaving actual operation of the bubble memory subsystems to the dedicated controller.

This section presents the 7225[2] bubble memory controller (BMC) and briefly describes the signals produced to control the functions of a bubble memory module, and the interface the controller presents to the external system accessing the bubble memory. These signals are depicted in Figure 2.7.

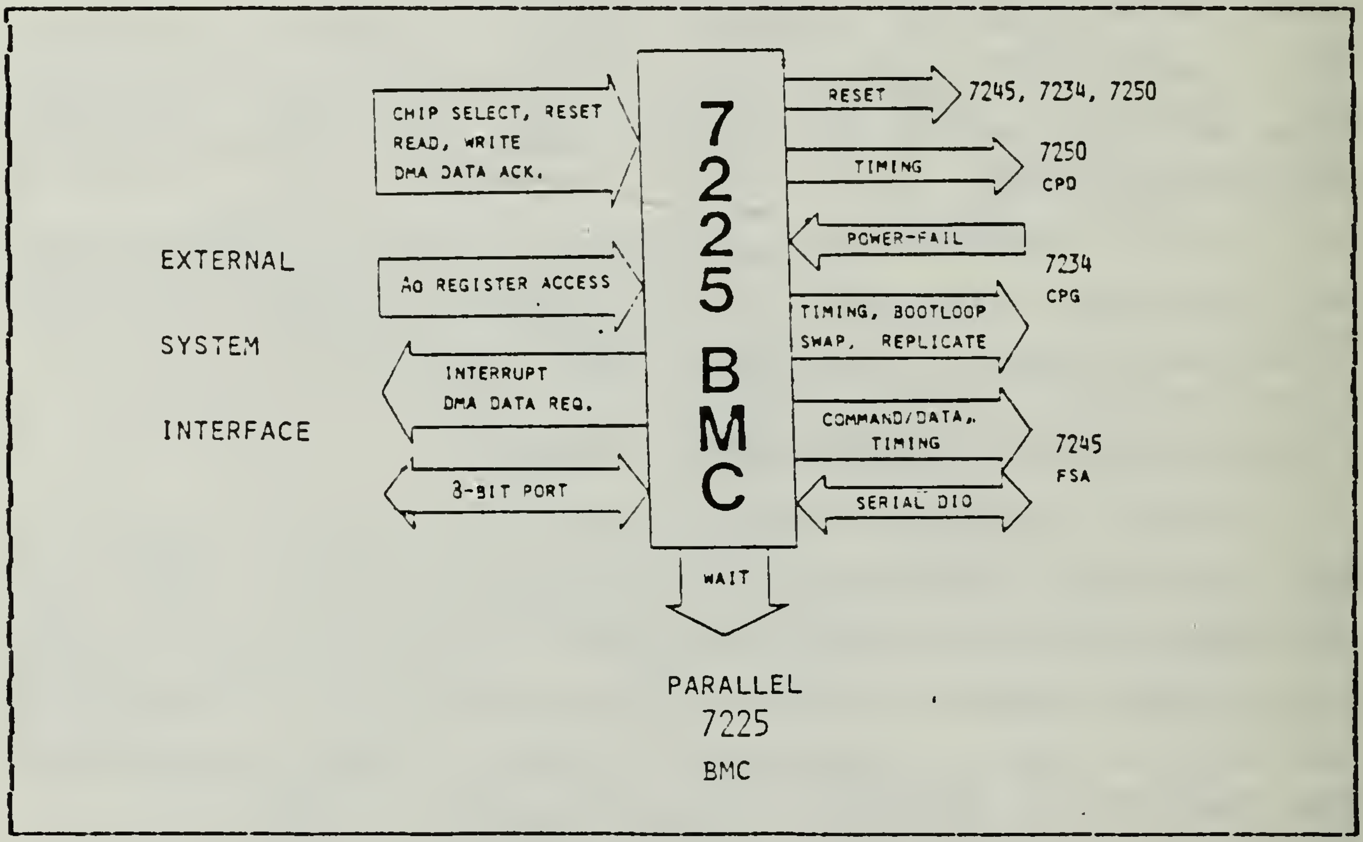

Figure 2.7 7225 Bubble Memory Controller Signals.

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[2] This section is based on information about the existing 7224 BMC chip and the expected capabilities of the 7225 chip as described in advance information provided by Intel. See Appendix B.

1. Bubble Memory Signals

Descriptions of the signals that pass between the controller and support chips have been provided in the component descriptions of the last section. Figure 2.7 summarizes the memory component control signals associated directly with the bubble memory controller. Most important are the critical timing signals provided to coordinate the bubble memory functions with respect to movement of the magnetic bubbles with the rotating magnetic field. The controller also exchanges command, status, and data signals to the memory module via the 7245 FSA, and produces swap and replicate signals and receives power-fail indications directly with the 7234 CPG.

2. External System Interface

The interface to the external system consists of memory access function lines and an eight-bit data bus as shown in the figure. The function lines are compatible with other Intel controllers and their interconnections with other types of data storage systems. The user must send specific bubble memory commands over the interface to the bubble memory controller to prepare the system for data input or output before each accessing operation. Chapter 3 discusses the interaction process required by an external system in accessing a magnetic bubble memory.

When these commands are received, the BMC generates the required signals to the memory cell components to perform the operation with no further intervention by the external system required besides the necessity to provide or accept data at a known rate.

The external system can either transfer data directly with the BMC using a polled status mode to coordinate data flow, or incorporate a direct memory access (DMA) system to manage handshake protocol with the BMC separately. The polled mode is simpler to incorporate but requires constant attention by the external system to manage data flow. DMA relieves the external system of this requirement, but incorporates additional hardware and increases system complexity. The method employed would depend on the particular application (required data rate) and the specific external system involved.

The process of determining the operational memory configuration best suited for a particular recording need is outlined in Chapter 4. A sample system is presented in Chapter 4 as well, but since there are many external system configurations which could provide the required interface to the magnetic bubble memory, no specific discussion of external systems or suggested data transfer method is presented in this paper.

3. Parallel Controller Capability

The "wait" signal is used to coordinate the actions within a magnetic bubble memory system using two 7225 BMCs actively transferring data simultaneously in parallel. The advantage of this capability is discussed later in this chapter.

4. Internal Operations

Internal operations of the bubble memory controller are described in detail in Appendix B. However, certain aspects of the internal configuration of the chip must be presented here in order to understand the system operation described in the next chapter. These aspects are also important to expansion of the system into a larger capacity configuration.

a. Power Failure, Abort, and Reset Logic

In the case of a power failure detected by the 7234 CPG or an externally-generated abort/reset signal, a routine is automatically initiated to de-activate the memory module in an orderly fashion to ensure data integrity within the magnetic bubble memory chip.

b. Internal Registers

A number of registers are accessed by the external system to prepare the memory system for operations. The registers specify the operation to be conducted, the amount of data to be transferred, the memory module and location within to be accessed, and the method to be used in the transfer. A register is also used to report the status of the operation and the occurance of any errors or complications. The registers are accessed via the eight-bit port using specific signals sent by the external system over the memory access lines. Operation of the bubble memory system includes frequent interaction with the BMC registers and this important process is described more fully in the next chapter.

c. FIFO

The 7225 BMC FIFO is a 128 x 8 bit first-in/first-out RAM used as a data buffer between the bubble memory and the external system. The magnetic bubble memory chip transfers data only in 64-byte blocks ("pages"), thus a full BMC FIFO may contain enough data at any one time for two complete transfers to a single memory module. Data are transferred between the BMC FIFO and the memory system at a fixed rate depending on the number of modules within the system. The average data transfer rate to a single memory module is 16 kbytes per second, two modules in parallel require 32 kbytes per second, etc. The BMC FIFO relieves any small differences in data transfer from the external system to the memory as long as the difference does not eventually deplete or overflow the data buffer before the operation is complete.

5. A Four-Megabit Magnetic Bubble Memory System

Figure 2.8 is a block diagram of a complete magnetic bubble memory system capable of storing up to four-megabits of digital information. The figure depicts the basic interconnections between a single memory module and the bubble memory controller which also serves as the interface to the external system accessing the bubble memory system. Though not labelled, the arrows between components represent the same associated signals as described earlier in this chapter.

C. MULTIPLE MEMORY MODULE SYSTEMS

1. Multi-Module Interfacing

Figure 2.9 shows how the basic system of Figure 2.8 is expanded to incorporate multiple memory modules into a system controlled by a single 7225 bubble memory controller. As can be seen, each module in the system receives the same BMC signals as are sent to a single module with the addition of a signal sent between the FSAs themselves. This signal establishes the time-multiplexing of the FSAs that allows the bubble memory controller to access multiple memory modules in a logical manner. This method of communication between the bubble memory controller and multiple FSAs is described in detail in Appendix B. Basically, the time-multiplexing scheme allows the BMC to establish communications with any single memory module, or with several combinations of modules in parallel operation, without

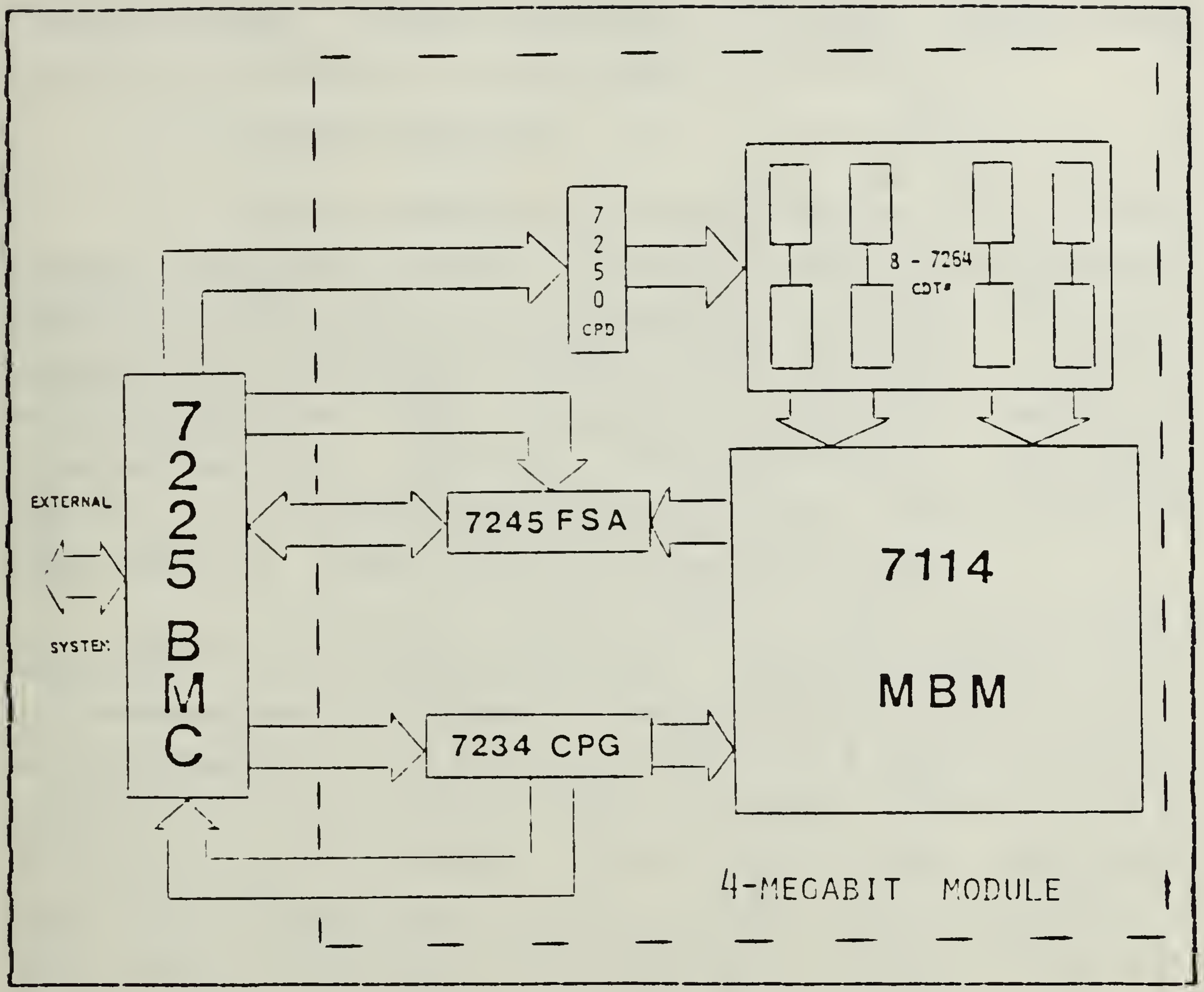

Figure 2.8 Four-Megabit Magnetic Bubble Memory System.

experiencing contention over the command and data lines common to all the modules. This communication scheme also accounts for the system performance characteristics associated with the different multi-module configurations presented next.

2. Multi-Module Operations

A single bubble memory controller physically connected to multiple memory modules is capable of accessing the modules in a number of ways, each of which produce different performance of the system in terms of data

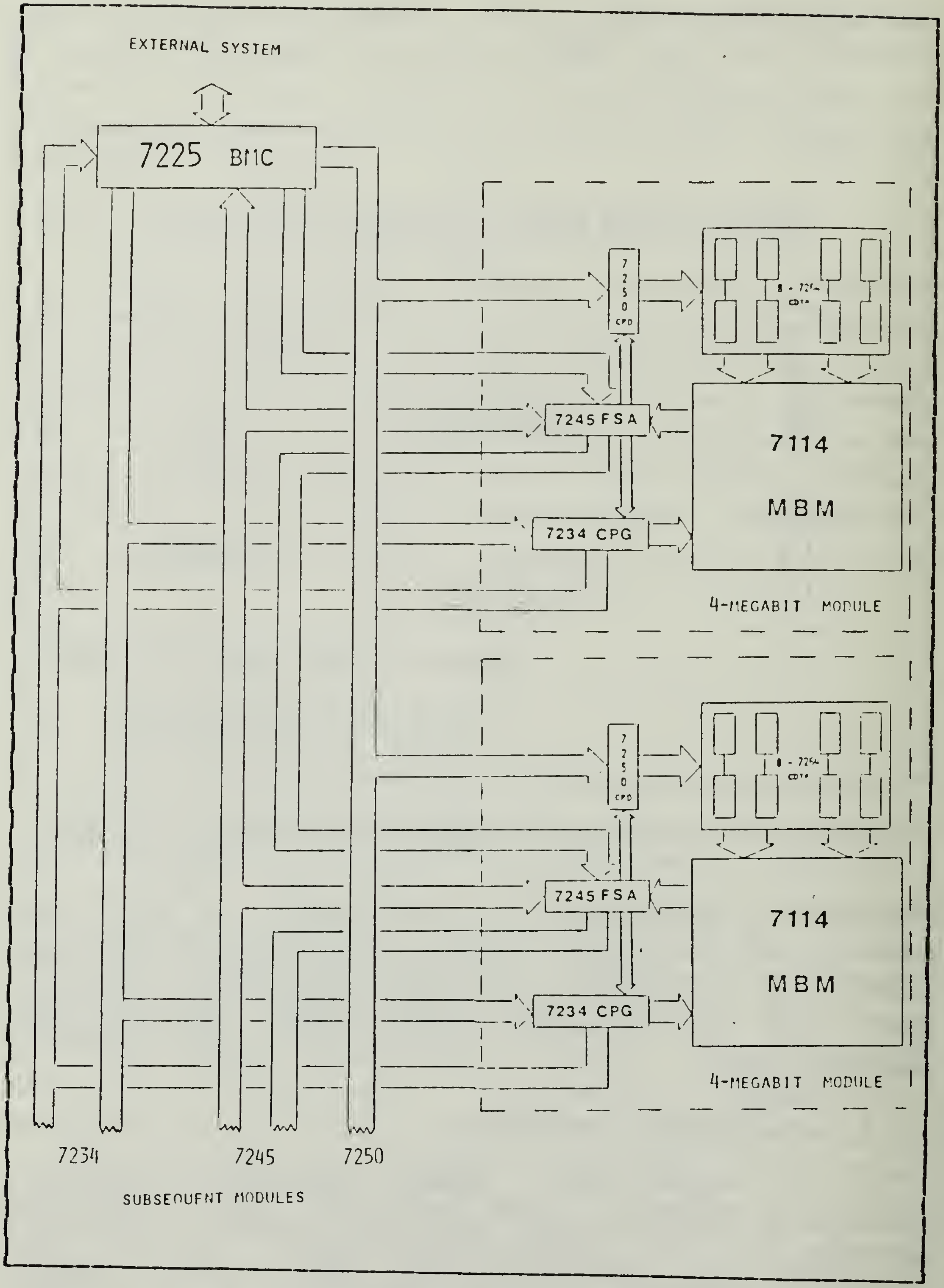

Figure 2.9 Multiple Memory Module System Configuration.

transfer rates. System capacity, of course, is determined merely by the number of memory modules incorporated.

a. Serial Operation

Serial accessing of memory modules by the bubble memory controller involves use of only a single memory module at a time for a given operation. The BMC establishes communication with the specific module FSA only, which in turn enables the other components within the module as required for data transfers. Other modules in the system are in a stand-by mode and ignore the BMC signals sent out over the lines common to all the memory modules.

Since only a single bubble memory chip is being accessed, each transfer operation requires a minimum block of 512 data bits (64 bytes), corresponding to one data bit per storage loop within the 7114 MBM, for a single page data transfer with the system. Multiple-page transfers may be specified by the command received from the external system for a given operation and would involve exact multiples of this 512-bit data block. Average data transfer rate between the BMC and a single FSA is 16 kbytes per second.

Table 2 lists the important operating parameters for single module (serial) system operation. This is the performance of a single operating module even if it is part of a multiple-module system. The power requirements stated are based on a prototype kit provided by Intel and actual power requirements would probably be lower for a custom-designed system. A module on standby would be powered but not actually in the process of transferring data (active). Since magnetic bubble memory is non-volatile, data will be maintained within the system even if all power is removed.

TABLE 2

Serial Memory System Operating Parameters

Single transfer page size	512 bits
Average (sustained) data rate	16 kbytes/sec
Power requirements (typical)	
Active	6.5 W
Standby	2.4 W
Note: No power required for data storage only	

b. Parallel Operation

By addressing more than one of the FSAs in the multiple memory module system, the bubble memory controller increases the amount of data that must be transferred each operation, and increases the rate at which the transfer occurs.

Combinations of two, four, and eight modules can be accessed simultaneously resulting in average data transfer rates which are multiples of the rate associated with a single operating module.

Since data are being transferred to multiple magnetic bubble memory chips simultaneously, the minimum block of data required for each transfer operation is also a multiple of the 512-bit (64-byte) page size required by a single 7114 MBM.

Power consumption changes with multiple module configurations as well. The power consumed depends on the number of modules in the system, and on the number of modules actively engaged in data transfer or in the inactive stand-by mode.

Description of specific multi-module performances are withheld until the next section which describes the optimum physical combination of the bubble memory components described to this point.

D. THE EIGHT-MODULE MAGNETIC BUBBLE MEMORY BOARD

A single 7225 BMC is capable of providing signals to up to eight memory modules simultaneously. While smaller physical combinations are possible, the eight-modules per controller configuration offers the user more flexibility of operation than any other possible configuration. This configuration also represents the optimum combination of elements in terms of volume and weight which is a critical factor in space systems designs. For these reasons, discussions of digital data recorder designs presented in Chapter 4 specifically involve an eight memory modules per single controller configuration.

Physical connection to eight memory modules allows the controller to access the available memory systems in a number of ways to achieve a desired performance in terms of data transfer rate or memory capacity. The operational configuration chosen is dictated mainly by the desired data transfer rate. Expansion of any such system to meet increased storage capacity requirements involves simple incorporation of additional controller/module combinations to the existing system. This procedure is demonstrated in Chapter 4.

The following subsections summarize the performance parameters of an eight-module magnetic bubble memory system.

1. Memory Capacity

Eight four-megabit chips offer a user data storage capability of 4,194,304 bytes (eight-megabytes) or 33,554,432 bits of digital information.

2. Data Rates

Serial (individual) operation of the memory modules transfers data at an average sustained rate of 16 kbytes per second.

Parallel operation multiplies this rate by the number of active modules resulting in transfer rates of 32, 64, or 128 kbytes/sec corresponding to the 2, 4, or 8 simultaneously operating module configurations possible. The operating configuration chosen is determined by the maximum data input/output rates expected with system operation.

The desired transfer rate is easily changed by the external system through the commands and operation specifications sent to the bubble memory controller via the external interface. This process is described in the next chapter.

3. Transfer Page Size

512 bits, corresponding to one bit for each storage loop, must be transferred into or out of each active memory module for a single transfer operation. Parallel module operation multiplies this page size by the number of modules involved in the transfer.

Table 3 summarizes the data transfer rates and minimum data page size required for a single transfer operation for each of the possible operating configurations of an eight-module memory system.

4. Power Consumption

As was indicated in Table 2 , a single memory module actively engaged in data transfer consumes about 6.5 watts. Again, this is based on data available for an Intel-produced prototype kit and power requirements for a configuration as described herein would probably be somewhat lower. A single

TABLE 3

Eight-Module Memory Board Performance

Number of modules operating in parallel	1	2	4	8
Data rate (kbytes/sec)	16	32	64	128
Page size req. (bytes)	64	128	256	512

module on stand-by, (ie. powered but not involved in data transfer), consumes about 2.4 watts.

Based on the information above, Table 4 lists the expected power requirements of an eight-module memory board in its different operating configurations.

5. Size/Weight

Figure 2.1 at the beginning of the chapter depicted the size of the major components of the magnetic bubble memory system. Figure 2.10 shows the estimated size of a single memory module. The area shown in the figure is a good estimate of the space required by an entire module system including circuit elements such as resistors and capacitors not illustrated. The layout in no way suggests that this is the recommended positioning of the elements within a module. [Ref. 11] outlines suggested board layouts for single and multiple-module configurations for the one-megabit magnetic bubble memory system which is similar to the four-megabit system in most respects.

TABLE 4

Eight-Module Memory Board Power Requirements

Number of modules active	Number of modules stand-by	Power required
0	8	19.2 W
1	7	23.3 W
2	6	27.4 W
4	4	35.6 W
8	0	52.0 W

The 7264 coil drive transistors represent the "tallest" components in the system, extending approximately 4/5 inches from the surface of the board. Based on this information, it is estimated that an entire eight-module memory board could measure approximately 8" x 18" as shown in Figure 2.11. Multiple-board systems would require about 1-inch spacing.

The "board circuits" indicated on the figure include a voltage regulator circuit to ensure voltage levels within specified limits (Appendix B), circuitry to assist in power-fail detection, storage devices to maintain sufficient voltage levels after a power failure to implement the shut-down procedure, and other memory board support circuitry as may be required such as line drivers to ensure adequate strength of the controller signals on the common lines to all the modules, etc..

The weight of the board assembly has been estimated from the available BPK5V75A prototype kits (Appendix B)

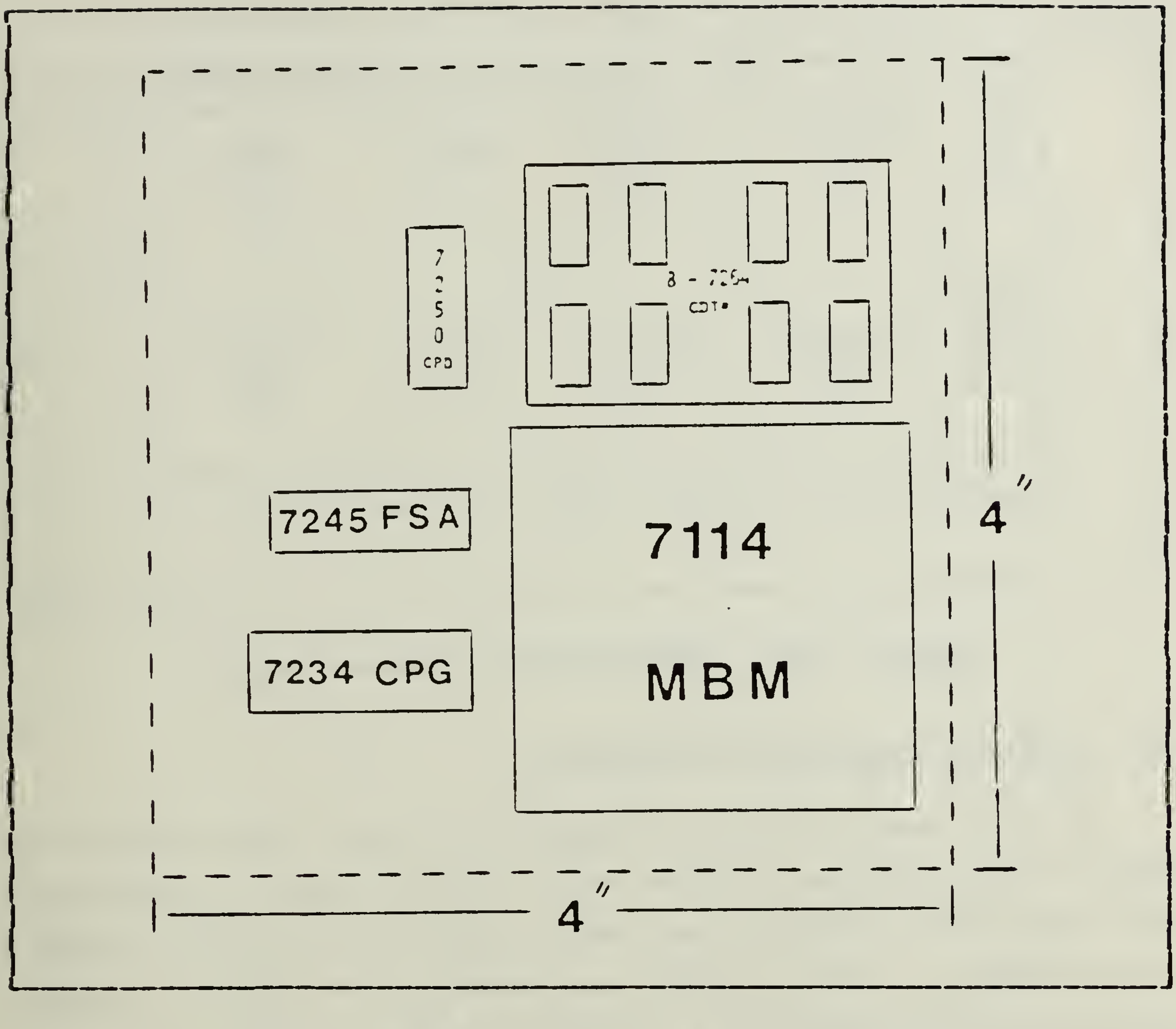

Figure 2.10 Memory Module Approximate Area.

which weigh 9.7 oz. each. Allowing for the weight of the extra components on the prototype kit not required on the memory board, the expected weight of an eight-module memory board would be approximately 43 oz. or less than three pounds.

It is the configuration depicted in Figure 2.11, and the operating parameters presented above, on which the discussion of a digital data recorder for space-based applications presented in Chapter 4 is based.

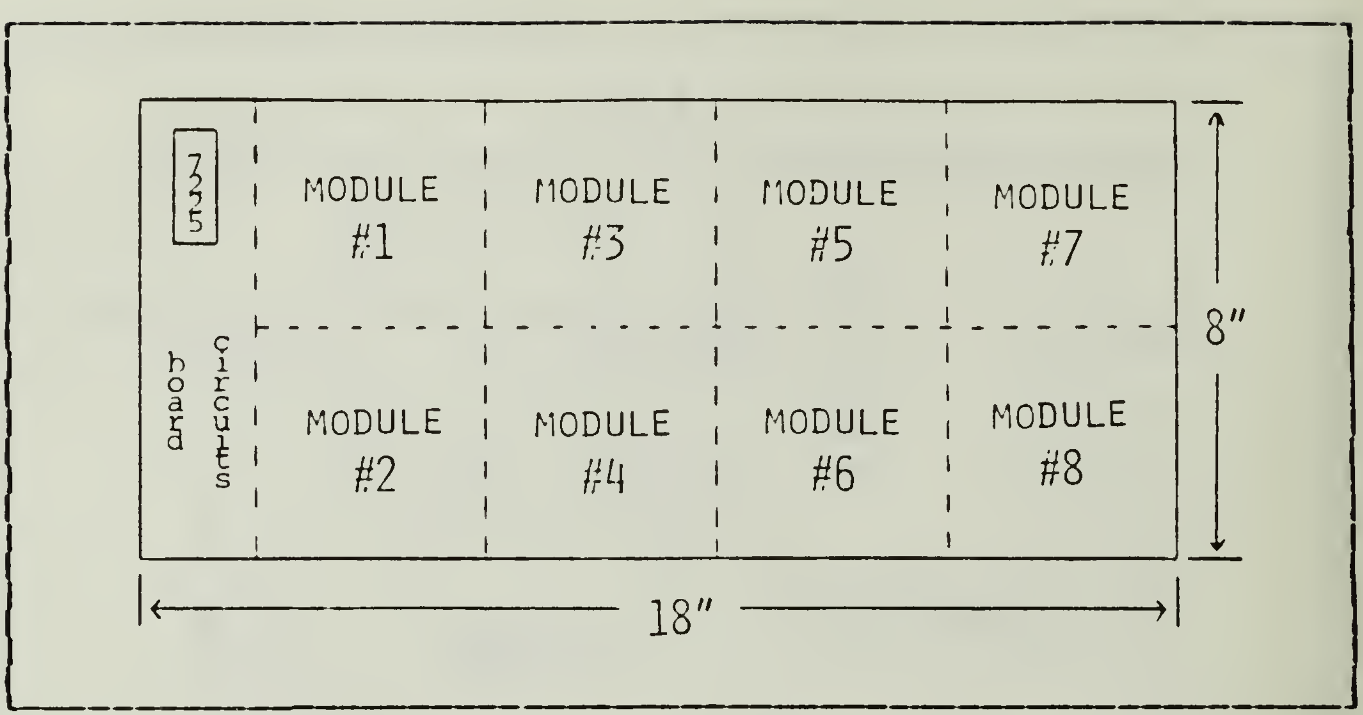

Figure 2.11 Eight-Module Memory Board.

E. PARALLEL CONTROLLER OPERATION

As was shown earlier in Figure 2.7 , the 7225 BMC has an output line labelled "wait" which can be used to coordinate the operations between two bubble memory controllers working in parallel. The two BMCs may operate two separate memory systems simultaneously to offer the user a 16-bit external interface capability. This would double the operating performances described for the system configurations described earlier.

The "wait" signal between the bubble memory controllers is used to ensure simultaneous operation of the systems during data transfers. In the case of a transfer delay due to a discovered data error (Chapter 3) or a power failure or reset signal within one of the memory systems, the signal would be passed from the delayed controller to the other system to inhibit further data transfer until the delay is corrected and simultaneous operation can be re-established.

Parallel system operation could be the topic of another bubble memory system study at the Naval Postgraduate School and will not be considered further in this paper.

III. MAGNETIC BUBBLE MEMORY SYSTEM OPERATION

This chapter describes the basic interactions between an external system and the bubble memory controller required for communication and data transfer. The information presented is a summary of information provided in [Ref. 12] and specifically emphasizes the procedures pertinent to a multiple memory module system as described in the last chapter operating as a digital data recorder. Though [Ref. 12] is provided as a guide to users implementing the BPK5V75A four-megabit Intel prototype kit, familiarity with the information therein is imperative before attempting to formulate the operating routines to be implemented by any external system utilizing the Intel four-megabit magnetic bubble memory systems in any operating configuration.

The routines formulated depend on the external system and data transfer method implemented as well as on the number of modules in the system. While no particular system or method is specified in this paper, differences in operation due to these factors is presented as they occur in the discussion.

Basically, the external system accesses the memory by sending specific operating parameters and command codes to the bubble memory controller which then produces the internal signals necessary to conduct the desired operation. If the operation involves data transfer, the system must provide or accept data at the rate and in the quantity that is specified by the operating parameters provided to the bubble memory controller by the external system prior to the operation.

The first section presents the method the external system uses to initiate the available functions of the bubble memory system. Combining these functions into a working operating routine is discussed in the following section.

A. BMC - EXTERNAL SYSTEM COMMUNICATIONS

The last chapter described the physical connection between the 7225 BMC and an external system as consisting of an 8-bit data bus and a number of memory access function lines. Figure 2.7 is repeated here to emphasise the external system interface. The interface shown is the same whether the BMC controls a single memory module or many.

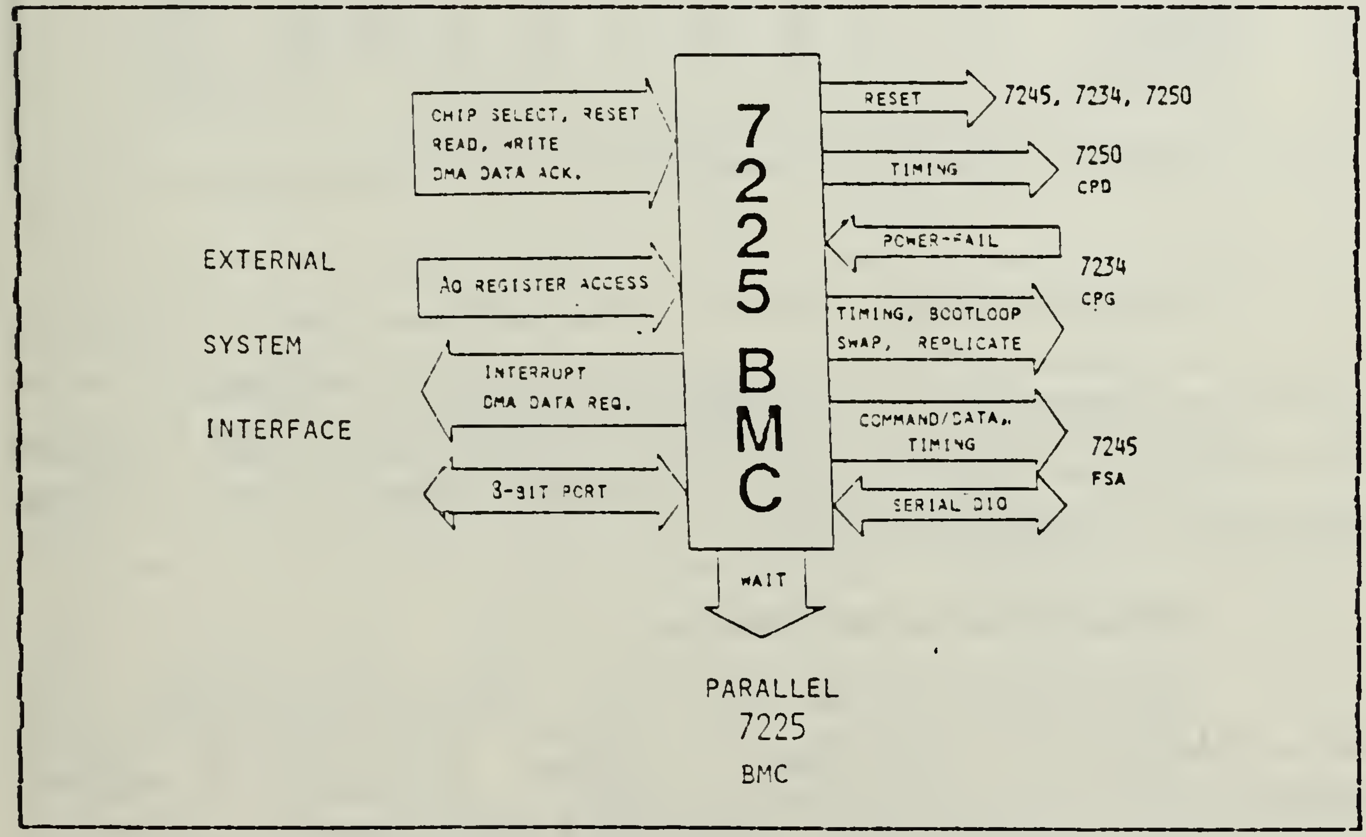

Figure 3.1 7225 BMC - External System Interface.

1. Command/Status Port

The command/status port consists of the 8-bit data lines, the A0 line, and the (separate) read (RD) and write (WR) lines as shown in table 5. Notice that the 8-bit data bus D4 bit line also plays a role in BMC communications.

TABLE 5

Command/Status Port Functions

Function	D7	D6	D5	D4	D3	D2	D1	D0	RD/WR	A0
Command	0	0	C	1	C	C	C	C	WR	1
RAC	0	0	0	0	R	R	R	R	WR	1
Status	S	S	S	S	S	S	S	S	RD	1

Access to the port is selected when the A0 line is set to a logical "1". The three possible locations accessed are differentiated by the level of the D4 bit and the read (RD) or write (WR) lines. Functional description of these locations is presented next.

2. Register Address Counter

Since description of their purposes explains much about operation of the memory system, the register address counter and its associated registers are discussed first.

With A0=1, D4=0, and WR=1,[3] the external system gains access to either the BMC parametric registers or the BMC FIFO, depending on the address on the D3-D0 bit lines of the data bus. Table 6 lists the registers and their associated addresses.

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[3] The external system will usually incorporate an encoding or hardware logic to ensure that the RD and WR lines are never set high simultaneously, as this would provide conflicting signals to the bubble memory controller.

TABLE 6

Register Address Counter Assignments

Register Name	D7	D6	D5	D4	D3	D2	D1	D0	RD/WR
Block Length Register (LSB)	0	0	0	0	1	0	1	1	WR
(MSB)	0	0	0	0	1	1	0	0	WR
Enable Register	0	0	0	0	1	1	0	1	RD/WR
Address Register (LSB)	0	0	0	0	1	1	1	0	RD/WR
(MSB)	0	0	0	0	1	1	1	1	RD/WR
7224 FIFO	0	0	0	0	0	0	0	0	RD/WR

NOTE: For all of the above, A0 = 0

Notice that the registers are addressed in hexadecimal order from 0BH to 0FH and that the FIFO has an address of all zeros. This arrangement is designed to allow the user to use an auto-incrementing feature of the RAC. After a particular register is addressed, and the associated byte transferred, the RAC automatically increments to the address of the next register in sequence to simplify the process of loading the operating parameters into subsequent registers. This process continues until the RAC rolls over to zero to address the BMC FIFO where it remains until a new valid address is sent to the RAC. This feature automatically prepares the memory system for data transfers after the parametric registers are loaded. Operations which do not require updating of subsequent registers may be performed as well, but require the external system to address the desired registers and FIFO separately as needed. After a specific register (or the FIFO) is addressed, lowering the A0 line allows data transfer with the register (or the FIFO on a bit-by-bit basis) depending on the level of the read (RD) or write (WR) lines. Note that the block length register may only be written into while the bytes associated with the other parametric registers may be read by the external system as well.

3. Parametric Registers

The parametric registers are used by the external system to specify the memory module(s) to be accessed, the amount of data to be transferred, the method of transfer to be used, and any error correcting scheme to be implemented. Normal system operation involves transfer of the operating parameters to the parametric registers (if required by the upcoming operation) followed by issuance of the command code to be executed. Once a command is issued to the BMC, the parametric registers must not be modified until the operation is completed or terminated as they are used as working registers by the BMC during command execution.

a. Block Length Register

The block length register is made up of a least significant byte (LSB) and most significant byte (MSB) as addressed through the RAC (Table 6). The bubble memory controller interprets the data in these two bytes as shown in Figure 3.2.

(1) Channel Field. Bits D7-D4 of the MSB are known as the channel field and specify the number of FSAs to be accessed during the next operation. Each FSA has two channels associated with each half-system of the bubble memory chip it services (Appendix B). To preclude

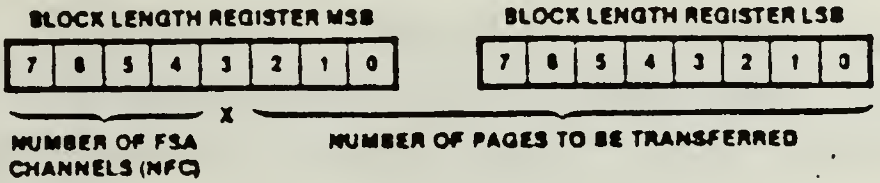
BLOCK LENGTH REGISTER MSB
7
6
5
4
3
2
1
0
BLOCK LENGTH REGISTER LSB
7
6
5
4
3
2
1
0
X
NUMBER OF FSA CHANNELS (NFC)
NUMBER OF PAGES TO BE TRANSFERRED

Figure 3.2 Block Length Register.

asynchronous operation of the channels within the memory chip, only one of the channel field bits may be set during a given operation. A channel field entry of 0001 would select only a single FSA (memory module) for the next operation. A 0010 entry would specify parallel operation of two modules simultaneously. The entries 0100 and 1000 would call for 4 module and 8 module operations respectively. A channel field entry of 0000 will allow half-system operation of a memory module, but this operation is included for diagnostic purposes only and is not a useful configuration in normal memory operations.

Thus, the entry in the channel field specifies the data transfer rate which will occur during the next data transfer operation, as well as the page size required for each single transfer. The channel field entry is also used to specify the particular memory module(s) to be addressed when combined with the MBM select field which is described shortly.

(2) Terminal Count Field. The D2-D0 bits of the MSB and the eight LSB bits combine to form the terminal count field. The eleven bits of this field are loaded with the binary number of total pages to be transferred during the next operation. This field limits the number of pages that may be transferred during a single commanded operation to 2048 pages.

b. Address Register

The address register also consists of a least significant byte (LSB) and most significant byte (MSB). The BMC interprets the data in these two registers as shown in Figure 3.3.

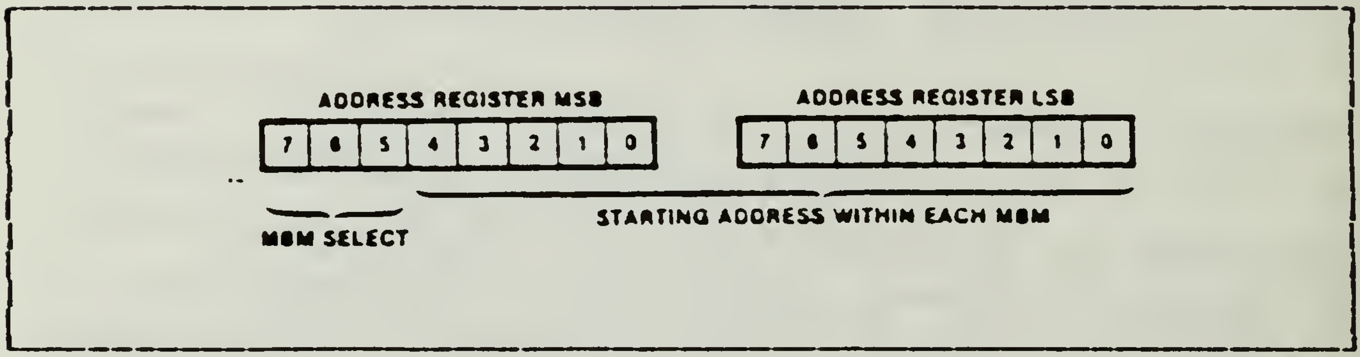

Figure 3.3 Address Register.

(1) Starting Address Field. The address register MSB D4-D0 bits and the eight bits of the LSB are interpreted as the logical page address within the memory module(s) at which the transfer operation will begin. The thirteen bits allow direct addressing of any of the modules' 8,192 storage pages. As each page of data is transferred, the starting address field is incremented to automatically select the next sequential page.

(2) MBM Select Field. Bits D7-D5 of the address register MSB are called the MBM select field. This field, along with the block length register channel field, specify the particular memory module or group of modules to be accessed. Table 7 illustrates this process.

For example, an MBM select field entry of 000 with a channel field entry of 0001 would address FSA channels 0 and 1 which are associated with the first memory module in sequence. An MBM select field entry of 001 with a channel field entry of 0010 would specifically address the

TABLE 7

Memory Module Addressing Scheme

MBM Select (Address Register MSB bits)	Channel Field (Block Length Register MSB bits)				
	0000	0001	0010	0100	1000
0 0 0	0	0,1	0,1,2,3	0 to 7	0 to F
0 0 1	1	2,3	4,5,6,7	8 to F	
0 1 0	2	4,5	8,9,A,B		
0 1 1	3	6,7	C,D,E,F		
1 0 0	4	8,9			
1 0 1	5	A,B			
1 1 0	6	C,D			
1 1 1	7	E,F			

second and third memory modules in sequence and call for parallel operation.

A useful feature of the address register is that when the starting address field increments past 8,192 , the MBM select field is automatically incremented as well to select the next sequential memory module or group of modules.

The address register(s) may be read by the external system. This allows the system to determine the stopping address within the memory for a recording operation of unknown length, and to specify the next page address as the starting point for the next recording operation.

c. Enable Register

The enable register specifies the data transfer method to be implemented, enables interrupt options, and specifies the actions the system will perform in the occurance of a detected data error. Each of the enable register bits shown in Figure 3.4 and their associated functions are discussed briefly.

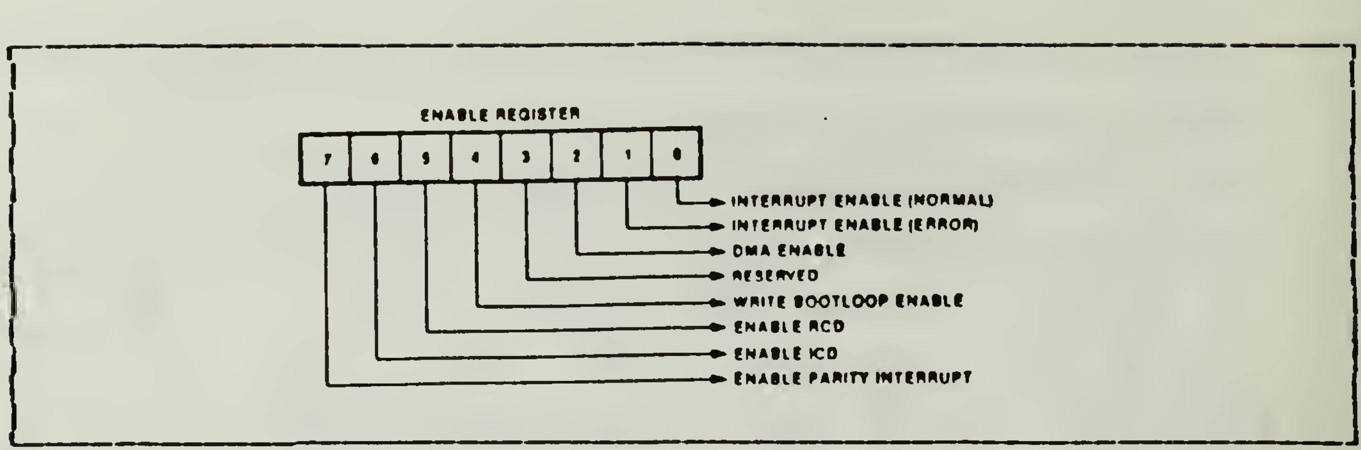

Figure 3.4 Enable Register.

(1) Interrupts. The bits D7, D1, and D0 enable the bubble memory system to produce an interrupt signal to the external system under certain conditions. The "normal" interrupt and the "parity" interrupt will not be incorporated in future Intel modifications of the systems. The external system should ensure that these bits are set to "0" each time the enable register is loaded.

The "error" interrupt enable bit (D1) is used in coordination with the read corrected data (RCD) and internally corrected data (ICD) bits (D5 and D6) to specify the level of error correction the system will implement and the actions the system will perform when an error is detected by the system FSA(s). The write bootloop enable bit is used to enable an external system to input data into the memory systems' bootloops. This action will not normally be taken by the user so the external system should also ensure that this bit is not set when loading the enable register. The D3 bit was associated with a function available with the one-megabit system and is reserved in the four-megabit systems. It also should be set to 0 at all times. Finally, the DMA enable bit (D2) when set allows the BMC to use its DRQ and DACK lines to establish a DMA handshaking protocol during data transfers with the external system. When not set, the system operates in the polled data transfer mode.

4. FIFO

The BMC FIFO is a first-in/first-out data buffer used to reconcile timing differences in data transfers between the external system and the bubble memory. The FIFO is dual-ported, allowing simultaneous input and output of data in a first-in/first-out method. Data transfer between the FIFO and the external system differs slightly with the data transfer mode selected. In the DMA mode the BMC uses the DRQ and DACK lines to establish a byte-by-byte transfer protocol with the external system. In the polled mode, the external system examines the FIFO READY bit of the BMC status register (described shortly) or the DRQ line signal level to determine when to transfer data to the FIFO. In either transfer mode, the external system must be capable of providing or accepting data at a sufficient rate to not allow the FIFO to deplete or overflow before the entire transfer operation is complete.

The FIFO in the 7224 BMC is 40 bytes long. Intel proposes to increase this space to 128 bytes (two full memory module pages) in its design of the 7225 bubble memory controller. This should increase the ability of the system to reconcile timing differences with the external system during data transfers.

5. Error Correction

The inherent data integrity of magnetic bubble memory systems is extremely high due to the physical architecture of the memory cell, and incorporation of error correction improves this integrity by several orders of magnitude. As mentioned in Chapter 2, the bubble memory systems' formatter/sense amplifier appends 28 bits[*] of error correcting code to each page of data input to its respective bubble memory for storage. The code is checked after the entire page is recovered from the memory before output to the bubble memory controller. If an error is detected, the FSA status register (Appendix B) is updated to reflect the type of error and subsequent memory system action depends on the level of error correction specified in the BMC enable register.

If a correctable error is detected, the FSA is capable of correcting single error bursts of five bits or less using the 14-bit appended error correction code and a built-in error correction algorithm.

The most common type of error occuring in magnetic bubble memories are "soft" read errors caused by noise in the bubble detection circuitry. Read errors do not affect the integrity of the data as stored in the memory chip and the error can usually be corrected by simply re-reading the affected page.

Table 8 lists the three available levels of error correction which may be implemented and the associated BMC enable register bit levels which specify the actions the system will take upon error detection.

In level 1 error correction, the RCD (read corrected data) bit is set in the enable register. When the FSA detects a correctable error with this level active, the BMC automatically issues a read corrected data command to the FSA which cycles the data through its ECC network and immediately transfers the data to the BMC. If the FSA status register still reports an error, the data transferred

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[*] 14 bits of error correcting code is appended onto each 256-bit half-page of data input to both FSA channels associated with each 7114 MBM. See Appendix B.

TABLE 8

Error Correction Levels

Error Correction Level	Enable Register Bit		
	Bit 6 ICD	Bit 5 RCD	Bit 1 Interrupt Enable (Error)
Level 1	0	1	0
Level 2	1	0	0
Level 3	1	0	1

are still erroneous and the BMC must interrupt the external system for further instructions.

When an error is detected with level 2 correction specified, the BMC first allows the FSA to cycle the erroneous data through its ECC network using the internally corrected data command to the FSA, and then checks the FSA status register to determine the outcome of the process before requesting data transfer using the RCD command. This halts the transfer operation at the erroneous page and allows the external system to mark the erroneous page and attempt re-reads and re-corrections through specific bubble memory controller commands.

When level 3 error correction is specified, the external system receives an interrupt signal with each occurance of a detected error. With levels 1 and 2, corrected errors are transparent to the external system. Level 3 allows the external system to log all occurances of error detection and gives the system added ability to cope with multiple errors which may occur with multiple memory module system operations. It also requires additional routines to meet the additional responsibilities.

6. BMC Status Register

When A0=1 and RD=1 the external system receives an 8-bit status word from the BMC as shown in Figure 3.5. The status register provides information on the completion or termination of an operation, error occurance, and ability of the FIFO to accept or provide data. The external system uses the information from the status register to continue with normal operation of the memory system, or to implement routines to handle the occurance of errors.

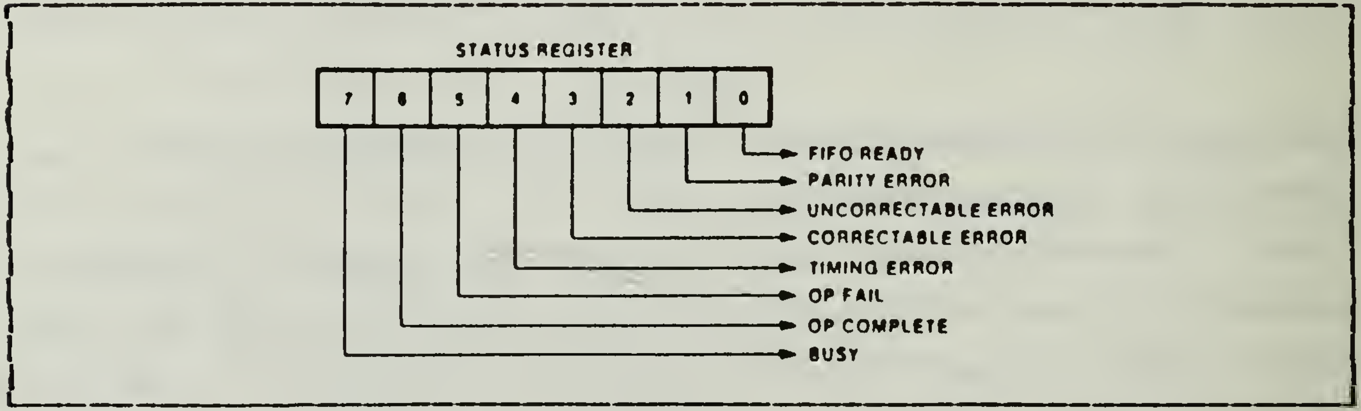


Figure 3.5 7224 Status Register.

When the BUSY bit is set, indicating an operation in progress, all other status register bits except the FIFO READY bit should be considered invalid. Only after the BUSY bit returns to 0 should the external system examine the status word to determine the outcome of the operation. Note also that while the BUSY bit is set, the BMC will not accept any new command except an ABORT command until the operation is complete or terminated.

When the BUSY bit returns to a low logic level, the external system examines the BMC status register to determine the outcome of the operation. If the OP COMPLETE bit is set, this indicates that the operation was completely and successfully executed. If the OP FAIL bit is set, the operation was not successfully completed and the external system will have to examine the other bits in the status register to determine the cause of the failure and the necessary actions to continue operation of the system.

7. Commands

When A0=1, WR=1, and D4=1, the D5 and D3-D0 bits of the data bus are decoded as a BMC command. Table 9 lists the available memory function commands and their associated command codes. Those commands marked with an asterisk are the most frequently used in normal memory operations. The others are either used less frequently or are for diagnostic purposes only. Since these commands are rarely used in normal operation of the bubble memory system, they are not considered here. [Ref. 12] gives a complete description of all the commands and their effect on memory system operation.

a. Abort

The ABORT command is the only command recognized by the BMC while it is in the process of executing a memory operation. For this reason, it is used whenever the system is in an unknown state, such as following power-up. If in the process of transferring data, the ABORT command terminates the operation and stops the MBMs in an orderly manner to ensure data integrity within the chip.

The ABORT command does not require any specific information to be loaded in the parametric registers before initiation.

b. Initialize

The INITIALIZE command prepares the memory system for operation when the system is in an unknown state. This command clears the address field of the address

TABLE 9

BMC Command Set

D5	D3	D2	D1	D0	Command
0	0	0	0	1	Initialize
0	0	0	1	0	Read Bubble Data
0	0	0	1	1	Write Bubble Data
0	0	1	0	0	Read Seek
0	0	1	0	1	Read Bootloop Register
0	0	1	1	0	Write Bootloop Register
0	0	1	1	1	Write Bootloop
0	1	0	0	0	Read FSA Status
0	1	0	0	1	Abort
0	1	0	1	0	Write Seek
0	1	0	1	1	Read Bootloop
0	1	1	0	0	Read Corrected Data
0	1	1	0	1	Reset FIFO
0	1	1	1	0	MBM Purge
0	1	1	1	1	Software Reset
1	0	0	0	0	Write Bootloop Register Masked
1	0	0	0	1	Zero Access Read Seek
1	0	0	1	0	Zero Access Read Bubble Data

register leaving the other parametric registers intact. The BMC FIFO and input/output latches are also cleared. The bootloop code of the memory module addressed by the MBM select (with the channel field specifying single module accessing only) is read into the BMC FIFO and then transferred to the FSA bootloop register. When the bootloop code is extracted the MBM is left positioned at logical page zero. In a multiple memory module system, the channel field must be loaded with 0001 to arrange accessing of the modules serially (separately), and the MBM select field must address the each module in turn to ensure initialization.

c. Read Bubble Data

This command initiates data transfer from the MBM(s) to the BMC FIFO. The parametric registers must be pre-loaded with the operating parameters before the command is issued.

d. Write Bubble Data

This command initiates the transfer of data from the BMC FIFO to the MBM(s) in the manner specified by the values pre-loaded in the BMC parametric registers. Note that data should not be loaded into the BMC FIFO until after the command is issued.

B. NORMAL OPERATING PROCEDURES

This section presents the methods of incorporating the commands described in the previous section in proper sequence for normal operation of the bubble memory system. The flow diagrams presented are derived from an earlier version of [Ref. 12]. The presently available systems require different operating procedures due to the hardware modifications incorporated by Intel to alleviate a problem which was limiting production yield (Appendix B). The methods presented here, derived from the earlier reference, more closely resemble the expected operating procedures which will be incorporated with systems based on the 7225 BMC and 7245 FSA.

The major operations illustrated are power-up, initialization, command execution, data transfer, and power-down. In each case, an algorithmic flow diagram of the operation is presented and remarks in amplification of the required commands already described is given.

1. Power-Up and Command Execution

Figure 3.6 describes the procedure used upon initial powering of the system. After applying power to the system, a 50-millisecond delay ensures that the system voltages have reached acceptable levels before commencing operations. The first command after applying power to a system is always the ABORT command. Notice that the BMC status register is

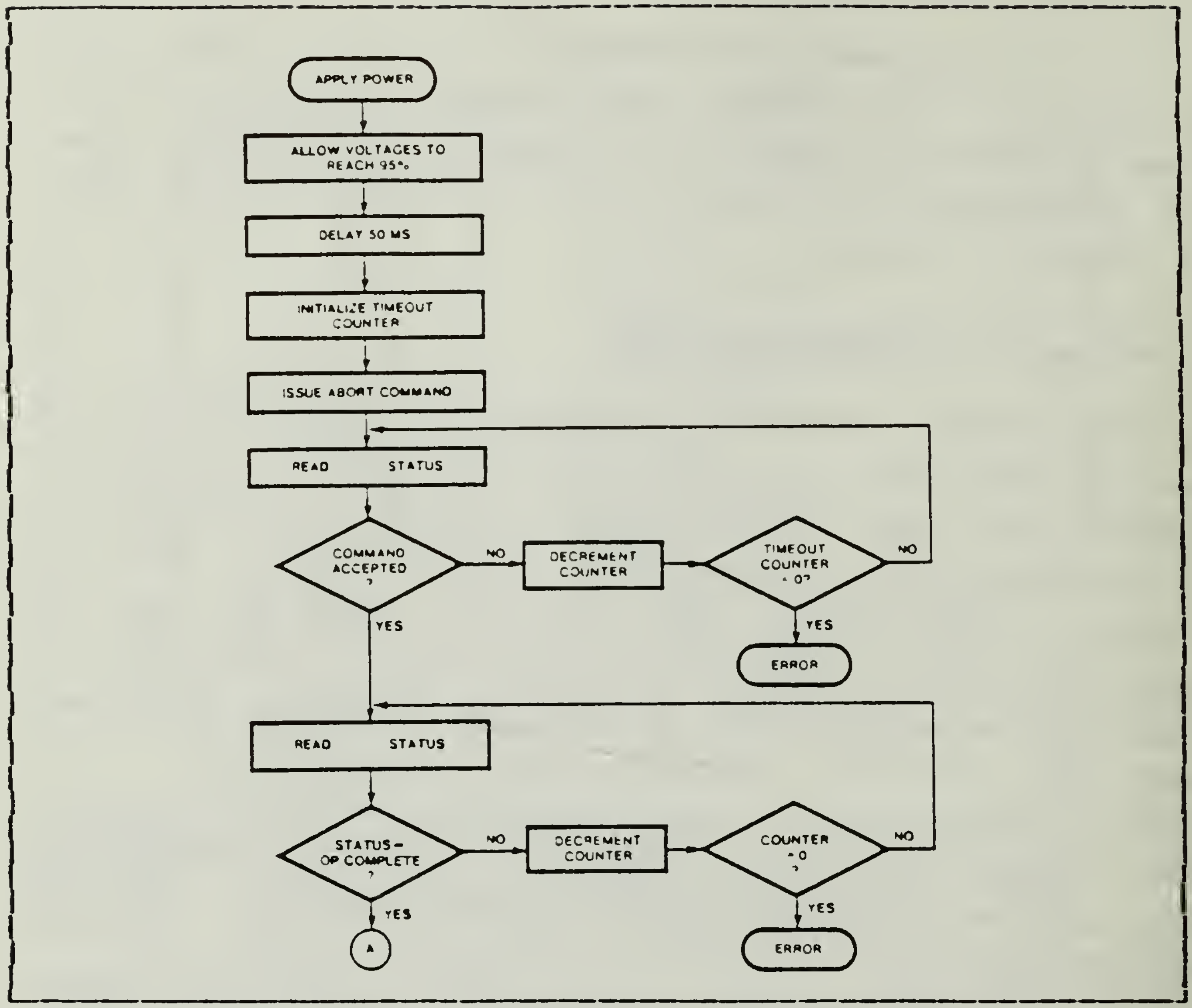


Figure 3.6 Memory System Power-Up Sequence.

examined first to determine that the command has been accepted (BUSY bit set), and then polled to determine completion of the operation. An external timeout counter is used to ensure operation within a reasonable period.

This process of issuing commands and examining the status register is the basic method used by the external system for execution of all the bubble memory functions.

Figure 3.7 shows the procedure used to perform the initiation of the memory system. Figure 3.8 illustrates the basic commands and logic used in general command execution.

The process used to transfer data with the bubble memory is shown in Figure 3.9 Besides illustrating the normal operating procedures of memory system operation, the flow diagrams also reveal the areas in which an error handling routine may have to be implemented.

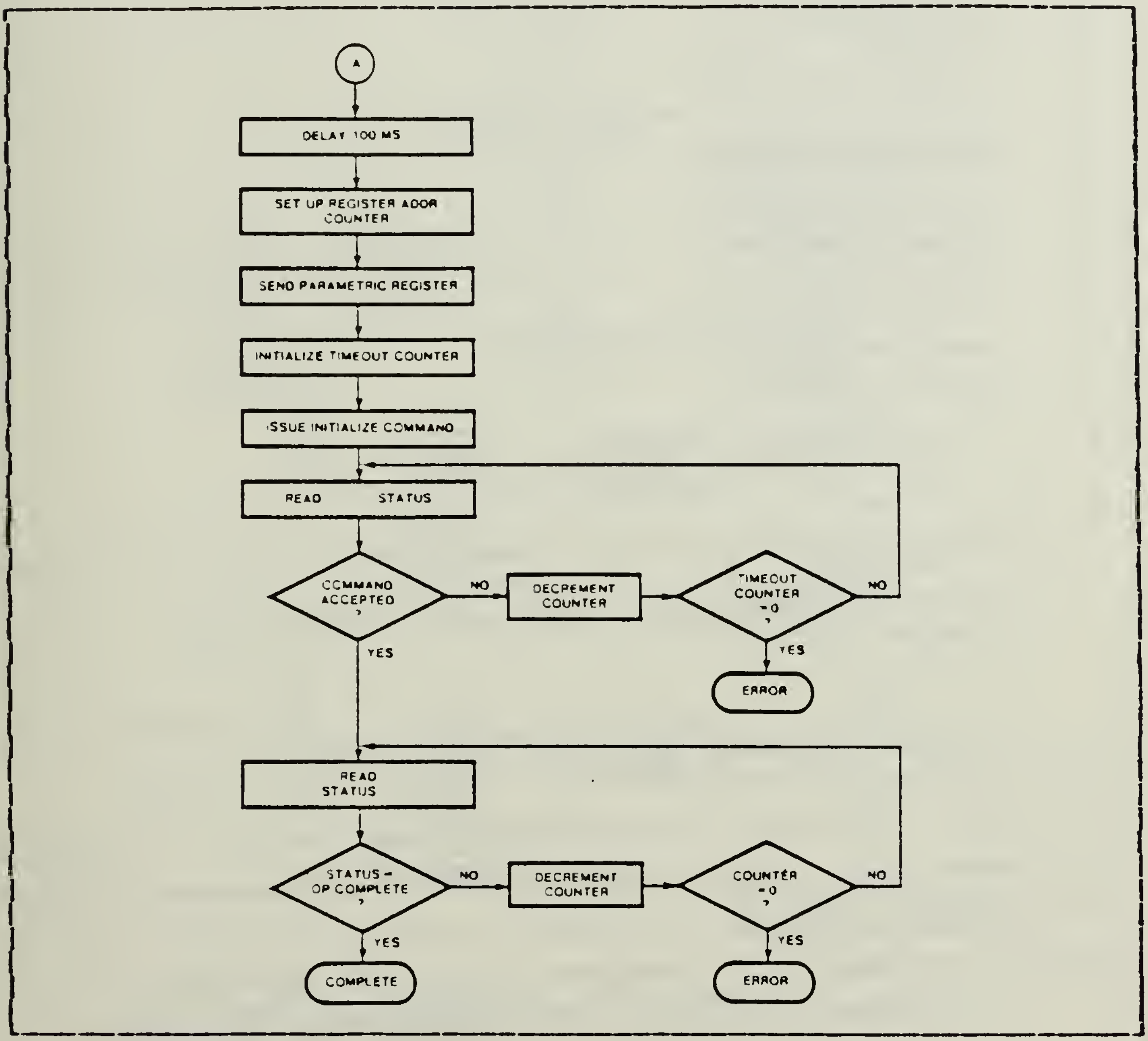


Figure 3.7 Memory System Initialization.

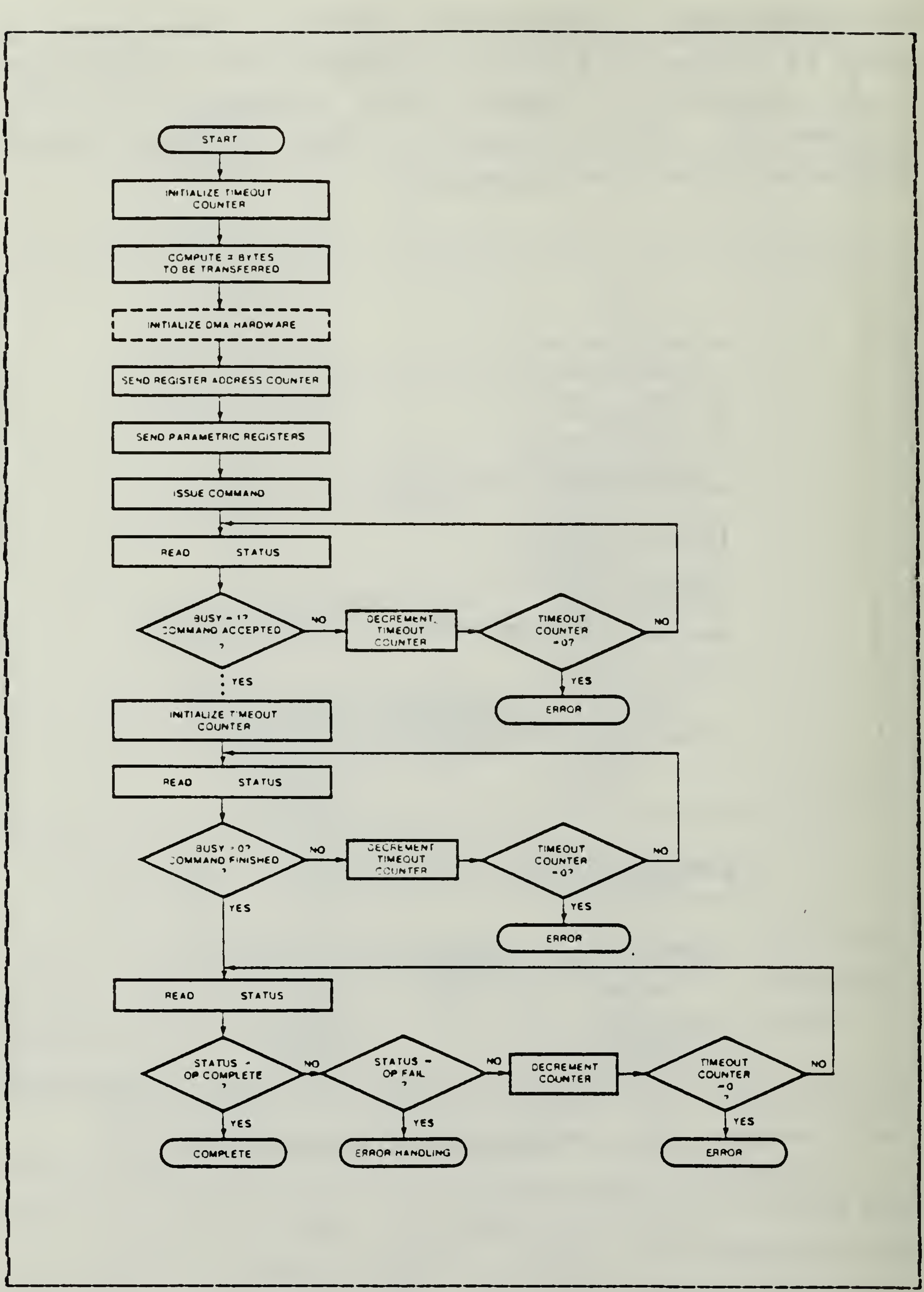


Figure 3.8 Memory System Command Execution.

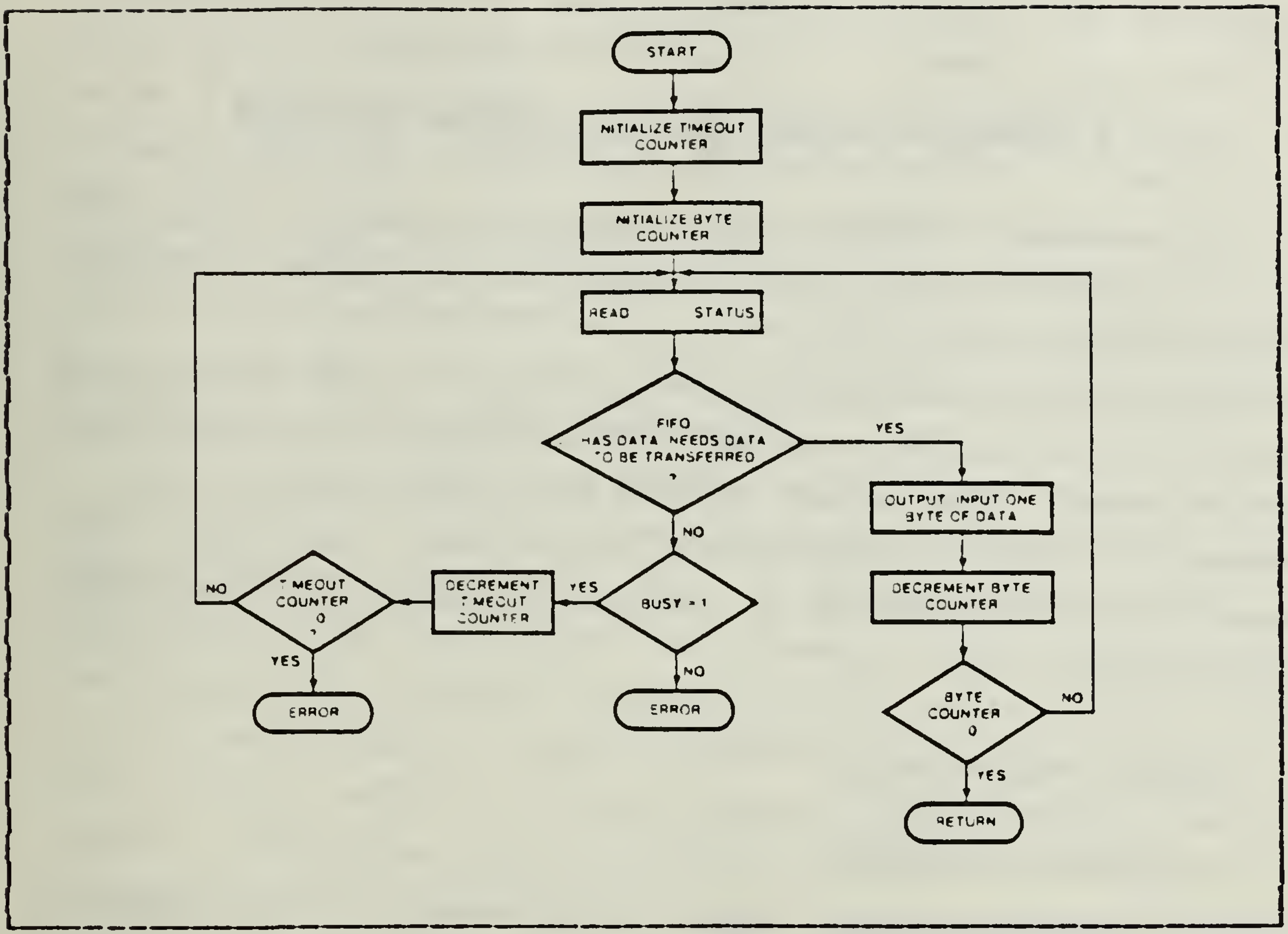


Figure 3.9 Data Transfer Procedure.

2. Power Down

Since the 7234 CPG incorporates power-fail circuitry, the shut-down procedure is the same whether the system is powered down intentionally or not. The power-fail circuitry includes storage elements to ensure adequate power to the system for the BMC to execute its shut-down routine and ensure data integrity.

IV. A MAGNETIC BUBBLE MEMORY DIGITAL RECORDER

This chapter describes the design process of a digital data recorder based on the eight-module memory "board" described in Chapter 2.

The first section describes the simple logic that can be used to determine the required system physical and operating configuration. The second section uses this design logic to propose a system configuration which could meet the data recording requirements of a space systems project currently in progress.

A. SYSTEM DESIGN LOGIC

1. Memory Capacity

The first factor to be considered is the amount of storage required for the particular application, which dictates the number of memory boards required by the system. The requirements should be computed in terms of numbers of pages to be input to the system for storage. Each single transfer operation requires 64 bytes of data for each operating memory module in the system. Incomplete pages of data may not be input to the memory. For example, storage of 20-megabits of digital information would require at least five four-megabit memory modules if the data could be configured to fill each of the modules completely during input.

2. Data Rate

The second configuration factor is establishing the data input/output rate to the bubble memory system. After the maximum transfer rate is defined, the operating configuration of the memory board is chosen to accommodate this rate. Differences between the transfer rates are buffered by the BMC FIFO but the external system must also ensure that the differences do not overflow or deplete the BMC FIFO during any specified transfer operation. The external system may incorporate a data buffer to ensure presence of sufficient data to accommodate the data transfer rate desired for a specified recording interval before initiating the transfer operation.

As an example, a single microphone connected to an 8-bit analog to digital converter being sampled 2000 times a second produces data at a rate of 16-kbits per second. The external system could elect to transfer this data, as it is collected, to a system operating its modules one at a time in the serial mode. Another option is to first collect the data into a buffer, in page format suitable for transfer, before initiating the transfer command to conduct the transfer at a faster rate using multiple memory modules operated in parallel. Multiple buffers may be imcorporated to ensure no loss of data as it is sampled. This buffering method is very useful when the data production occurs at a rate not compatible with memory system operation. After the required data rate is established, the capabilities of the external system to support this operation with the bubble memory recorder would determine the method of transfer to be implemented.

As an illustrative example of the configuration logic presented above, a proposed design of a digital data recorder based on a project currently in progress is presented in the next section.

B. N.P.S. PROTOTYPE DIGITAL RECORDER

1. Background

With the inception of two new curricula in Space Systems Engineering and Space Systems Operations at the U.S. Naval Postgraduate School, some of the officers involved pursued an idea of conducting an experiment as a space systems engineering/operations project. The National Aeronautics and Space Administration (NASA) offers space aboard the Space Transportation System (Space Shuttle) for experiments placed into a small, self-contained "Get-Away Special" canister (GAS can) which is carried into space within the shuttle cargo bay. Permission and funds were received to initiate an experiment to be carried inside one of these canisters.

2. Experiment Description

The experiment is designed to record the ambient acoustic levels within the shuttle cargo bay during launch. These data will be used to determine the acoustic modes, spectra, and levels within the bay as information to spacecraft designers to avoid potentially destructive acoustic coupling of structures or components carried into space aboard the shuttle.

Three microphones are used to record the acoustic information and three accelerometers furnish vibrational data. Each sensor is connected to an 8-bit analog-to-digital (A/D) converter to provide the recorder with digital information for storage.

The first stage of the experiment is accomplished by emitting a known signal into the loaded bay before launch and recording the responses. An acoustic signal is swept from approximately zero to 1000 Hz in one Hz increments which takes approximately 16.5 minutes. The second stage of the experiment records the ambient acoustic and vibrational levels during engine and rocket ignitions and lift-off. Only three minutes of operation are required to record the signals considered significant during this event.

3. Recorder Requirements

The sample rate for all sensors is fixed at 2.5 KHz. During the first portion of the experiment, only the three microphones are recorded producing approximately 7-megabytes of digital data for storage in the 16.5 minutes of the sound-sweep. During the second stage all six channels are recorded during ignition and lift-off, producing approximately 3-megabytes of information. Total memory capacity required therefore is around 10-megabytes.

Two different data input rates must be accommodated. Maximum data input rate occurs during the second portion of the experiment where operation of all six channels generates 15,000 bytes (15 kbytes) per second of information for storage. Three channel operation produces half this data rate.

4. BPK 5V75A Prototype Kit Design

Intel Corp. produces a four-megabit magnetic bubble memory prototype kit labelled BPK 5V75A which is a fully constructed magnetic bubble memory system on a single card. This kit is described in Appendix B and is basically comprised of a 7224 bubble memory controller and a modified single four-megabit magnetic bubble memory module. The kit was chosen for use due to ease of implementation and availability, and its applicability as a space systems experiment on its own merit.

A series of 24 BPK kits are installed in a box measuring approximately 14"x14"x15" consuming 2940 cubic inches or 1.7 cubic feet of volume. Weight is estimated at about

50 pounds and power requirements are expected to be around 20 watts.

Maximum data rate during lift-off is 15 kbytes per second as described earlier. DMA techniques have been incorporated for data input to the system, requiring additional components and hardware to the 24 BPK kits and the overall recorder controller which coordinates data flow to each of the prototype kits. Data is transferred to the memory chips serially from buffers which collect many pages of data before each transfer is conducted.

A complete description of the design, construction, and capabilities of this system is the subject of another thesis currently in formulation.

5. Multi-Module Custom Design

This subsection briefly describes the improvements which could be realized if the same system as described above was designed using the memory components configured on an eight-module memory board as described in Chapter 2. Only the capabilities and advantages of the memory board compared to the prototype kit design is examined. No specific external system or data transfer rate will be specified, although approximated system size, weight, and power consumption will be increased to reflect the requirements of these components within the system.

The initial sound sweep of the shuttle cargo bay produces data from the three microphones for a period of approximately 16.5 minutes. Each channel is sampled at a rate of 2500 times a second, producing 7500 bytes of information each second for input. In terms of pages, the data rate is 117.1875 pages per second. In integral numbers, 1875 whole pages of data are produced every 16 seconds. 16.5 minutes of recording would produce 116,015 whole pages of digital information (disregarding a fractional page recorded). This amount of data would require 14 complete memory modules and 1,327 pages of an additional module.

Two complete memory boards of 16 total memory modules exceeds the data requirement for this portion of the experiment and represents a logical and manageable apportionment of the memory system components.

During the second stage of the experiment, all six channels produce data, increasing the data rate to 15 kbytes per second, corresponding to 234.375 pages per second, or 1875 pages every 8 seconds. At this rate, a complete memory board records over 4.5 minutes of data which exceeds the specified requirements.

The proposed recorder design then, consists of three memory boards with an additional support circuit board included to incorporate the required external systems such as DMA hardware, data buffers, power regulators, etc.

Based on the characteristics described in Chapter 2, such a system would measure approximately 18"x8"x5" corresponding to 720 cubic inches, or less than one half cubic foot volume. Weight is estimated at about 12 pounds. This represents a significant improvement in these properties over the prototype kit design. Serial operation of the modules on the boards could easily accommodate the data transfer rates, though parallel operation in association with intermediate buffers is a possible operating option. Power consumption is similar to the prototype design of 20 watts.

It should be noted that in both designs, and in magnetic bubble memory system design in general, incorporation of a power switching circuit to supply power only to the memory modules actually engaged in data transfer will result in a significant reduction in power use [Ref. 13]. This takes advantage of the non-volatile property of magnetic bubble memory.

Construction of the proposed digital data recorder must wait for release by Intel of the updated version of the four-megabit magnetic bubble memory system including the 7225 bubble memory controller and the 7245 formatter/sense amplifier chips. These components will represent the optimum in size, weight, data density, and power consumption in magnetic bubble memory technology. Since these properties are of special concern to the space systems designer, future designs of digital data recording systems for space-based applications should consider the merits of the use of magnetic bubble memory.

APPENDIX A
MAGNETIC BUBBLE MEMORY TECHNOLOGY

A magnetic bubble memory is comprised of a substrate material in which magnetic bubbles are stored, and the structures and components that permit location and movement of the bubbles within the substrate and input and output of data with the memory. This appendix explains the basics of a magnetic bubble memory system and the support mechanisms required for proper operation.

A. MAGNETIC BUBBLE MEMORY CELL DESCRIPTION

The term "magnetic bubble memory cell" is used to describe the component within which magnetic bubbles are stored. This includes structures to locate and move the bubbles as well as the medium in which they are contained. Since this is the only area in which magnetic bubbles exist, the means for creation and destruction of magnetic bubbles is also described.

1. Substrate

The material in which the magnetic bubbles are stored is called the magnetic substrate and is usually a thin film of a synthetic garnet material with uniaxial ferromagnetic properties. Figure A.1 shows a section of substrate material with its inherent regions of opposite magnetization and shows the effect on these regions of an applied external magnetic field. Application of the field perpendicular to the garnet material axis of magnetization causes the areas of magnetization opposite to that of the applied field, known as the bias field, to compress.

Increasing the bias field eventually forces these regions to form stable, compact cylindrical shapes within the medium. These cylindrically shaped domains are the magnetic "bubbles" which will be used to represent stored digital data within the substrate.

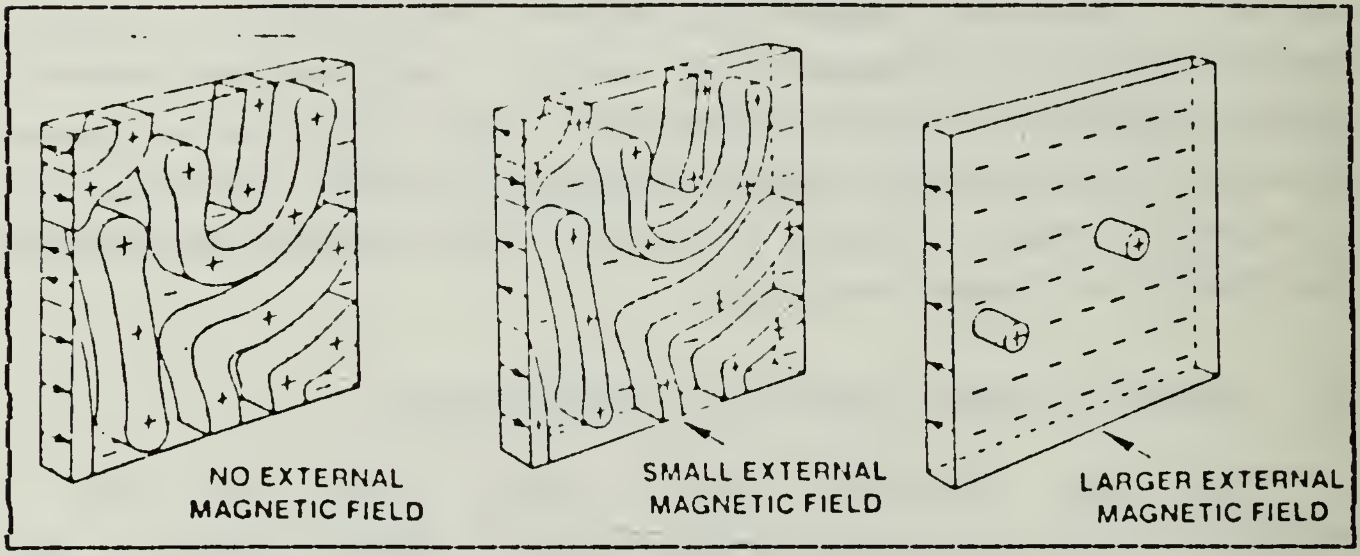

NO EXTERNAL MAGNETIC FIELD
SMALL EXTERNAL MAGNETIC FIELD
LARGER EXTERNAL MAGNETIC FIELD

Figure A.1 Magnetic Substrate and Effects of an Applied Perpendicular Magnetic Field.

2. Permanent Magnet

The size of the bubble domains is determined by the strength of the bias field. Strengths of 100 - 200 Oersteds produce useable bubble sizes and can be easily provided by permanent magnets superimposed around the substrate material. Barium or strontium ferrite magnets of 120 - 180 Oe are commonly used and result in bubble sizes of around 3 microns diameter. Once formed, the magnetic bubble domains remain preserved within the substrate as long as the bias field is maintained. Since no external power is required by the permanent magnets, memories storing digital data as discrete magnetic bubble domains within a substrate material represent non-volatile storage systems.

3. Location and Movement of Data Bubbles

To be useful, the magnetic bubbles which represent the stored digital data must be locateable and accessible.

a. Permalloy Structures

Each location within the substrate used to store a magnetic bubble is marked by a tiny permalloy (nickel-iron alloy) structure on the surface of the material. The wide-gap structures depicted in figure A.2 have been found optimum in terms of location and movement of the bubble domains within the substrate as well as in manufacturing considerations [Ref. 14]. As described in the figure, the shape and spacing of these structures is directly proportional to the magnetic bubble diameter established by the bias field. This defines the required minimum feature capability of the manufacturing process.

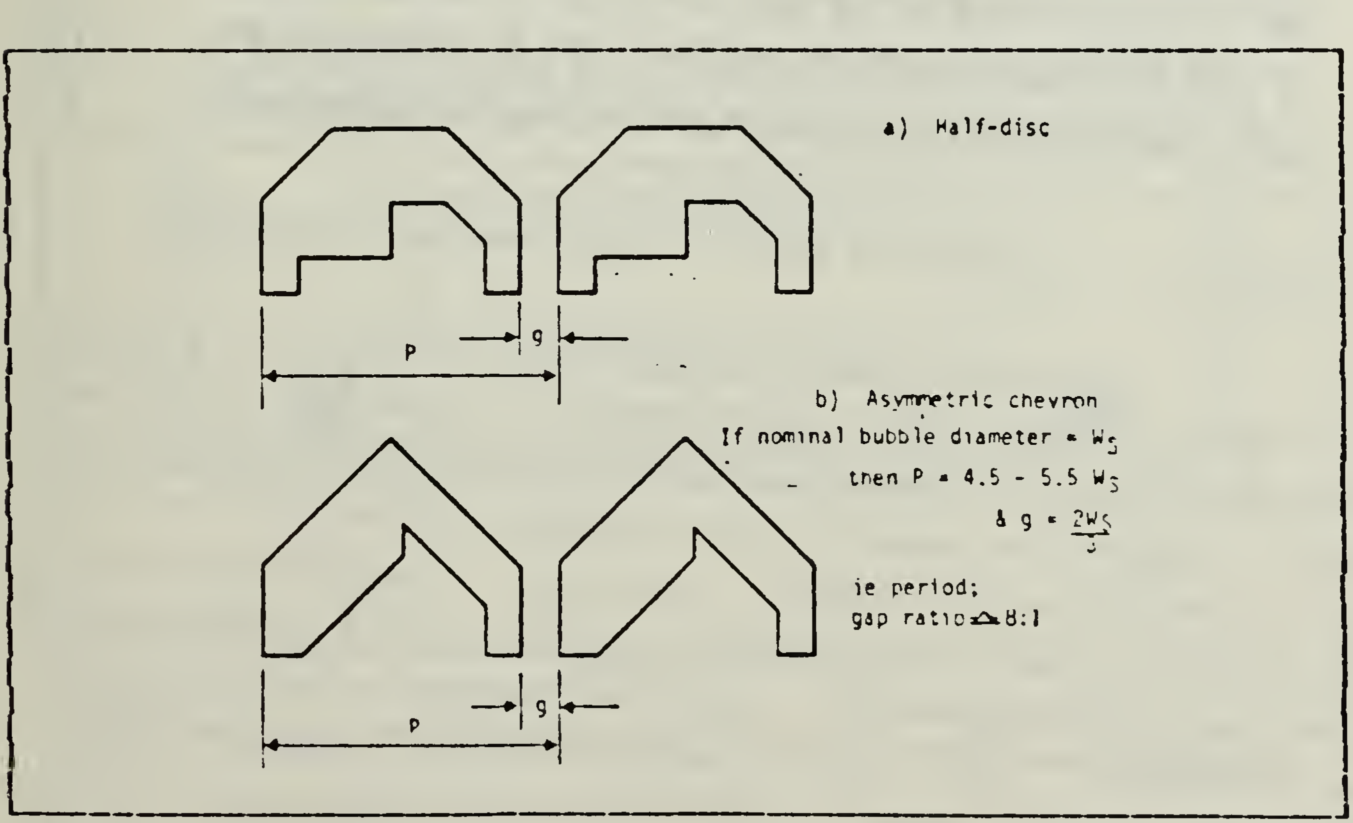


Figure A.2 Wide-Gap Permalloy Structure Designs.

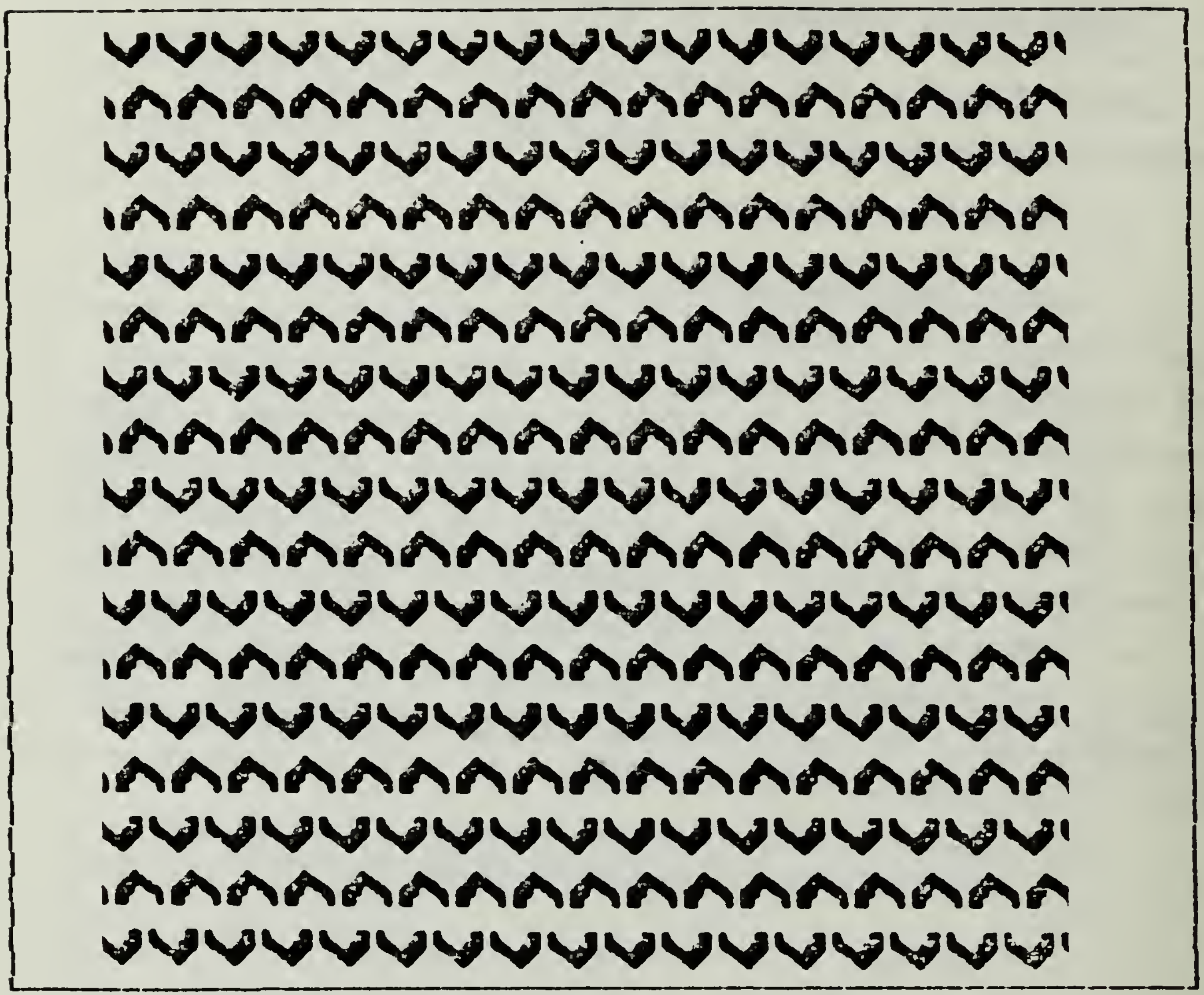


Figure A.3 Magnified View of Chevrons on Substrate.

Figure A.3 shows a magnified picture of a group of chevron structures superimposed onto a substrate material. Limiting factors to bubble capacity within a given area of substrate material are maximum intensity of bias field possible before bubble implosion (forced reversal of the magnetic field of the bubble domain), and the ability to create and superimpose the required storage structures onto the substrate. The first limitation is a property of the substrate material used, while the second limitation is due to the available manufacturing processes. Conventional UV photolithography minimum features are about 1 micron. X-ray lithography and ion-implantation techniques promise to reduce this even further allowing additional increases in capacity for the same area of substrate [Ref. 15].

When in the presence of an in-plane magnetic field, the permalloy material produces a magnetic component perpendicular to itself. This component adds to or subtracts from the bias field set up by the permanent magnets and produces "field wells" to which the magnetic bubble domains are drawn by the local magnetic gradient. A continuous in-plane magnetic component is provided by tilting the substrate material slightly to the plane of the permanent magnets as shown in figure A.4 . This establishes the storage location "field wells" occupied by the bubbles when the memory is inactive.

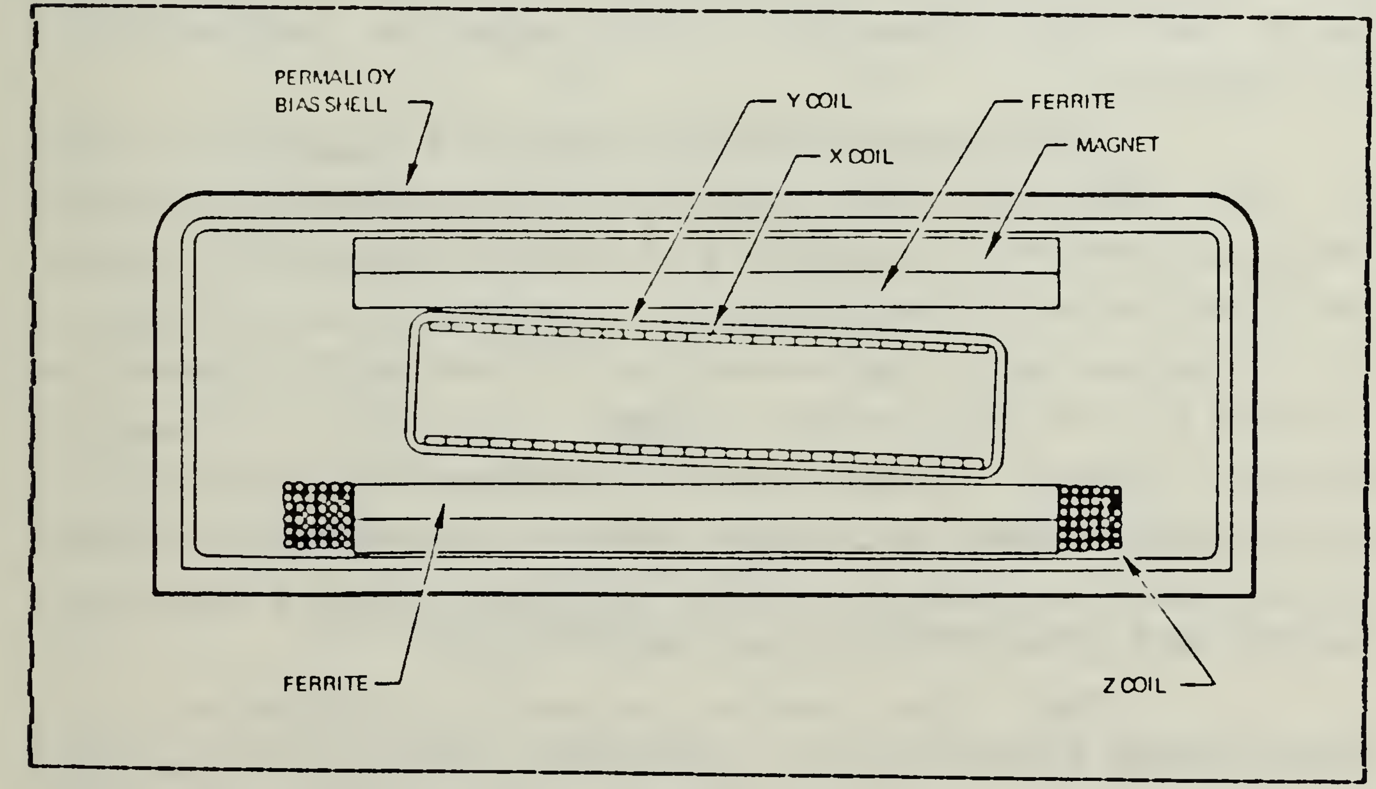


Figure A.4 Orientation of the Substrate and Magnets.

b. Rotating Magnetic Field

For movement and accessability of the magnetic bubbles, a rotating magnetic field is set up about the magnetic substrate by two perpendicular coils driven at a known frequency. See figure A.4 and figure A.13 at the end of this section for coil configuration within the memory cell. Sinusoidal currents oriented in quadrature through the coils produce a smoothly rotating magnetic field. The accepted method, however, is application of current pulses through Schottky diodes which produce triangular waveforms as shown in figure A.5 . Application of current pulses is easier to control digitally than application of sinusoidal signals and the resulting waveforms produce an acceptablly smooth rotating field vector. The timing of the pulses establishes the rate of rotation of the field which determines the rate of movement of the magnetic bubbles within the substrate.

The rotating magnetic field is oriented in-plane to the substrate and produces a perpendicular magnetic component from the permalloy structure as described earlier. The rotation of the applied field combined with the shape of the permalloy structure causes the "field well" beneath the chevron to move in a known manner. The change in magnetic gradient pulls a stored magnetic bubble along resulting in controlled movement of bubbles within the material. Figure A.6 is used to explain bubble movement between structures due tc an applied rotating magnetic field.

The first chevron in each row represents the same chevron viewed at five different times while the field is rotated about it. Each row shows three successive chevrons in what could be a line of associated data locations within the substrate. The arrows to the right of each row depict the rotating field vector set up at these discrete

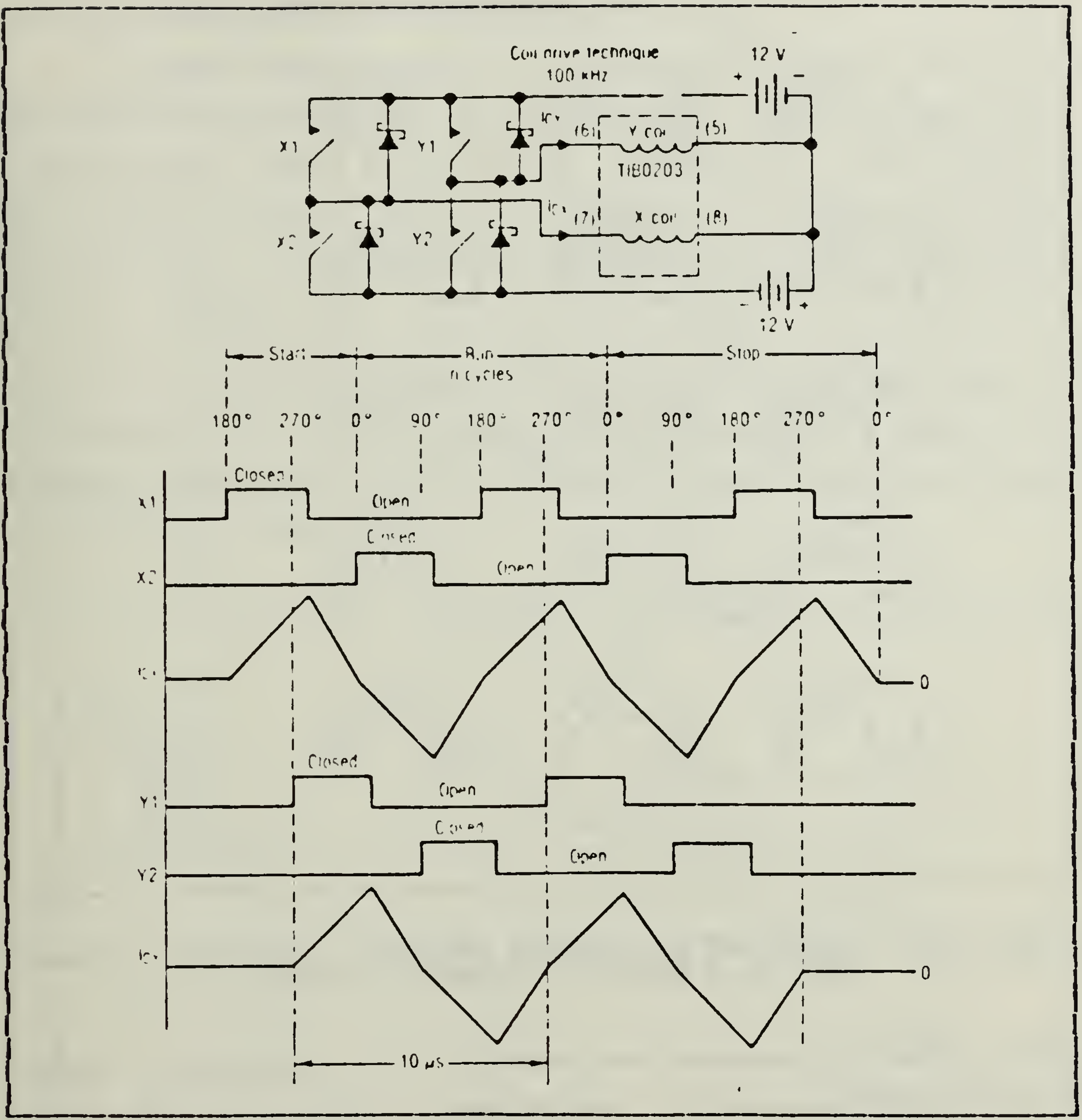


Figure A.5 Rotating Magnetic Field Circuit and Waveforms.

times by the perpendicular coils. Denoting the first row as having an applied vector of zero degrees, it can be seen that a bubble exists in position 1 beneath the first two chevrons and no data is stored in the third location. A shift of the rotating magnetic field vector by 90 degrees, depicted in the second row, moves the "field well" beneath

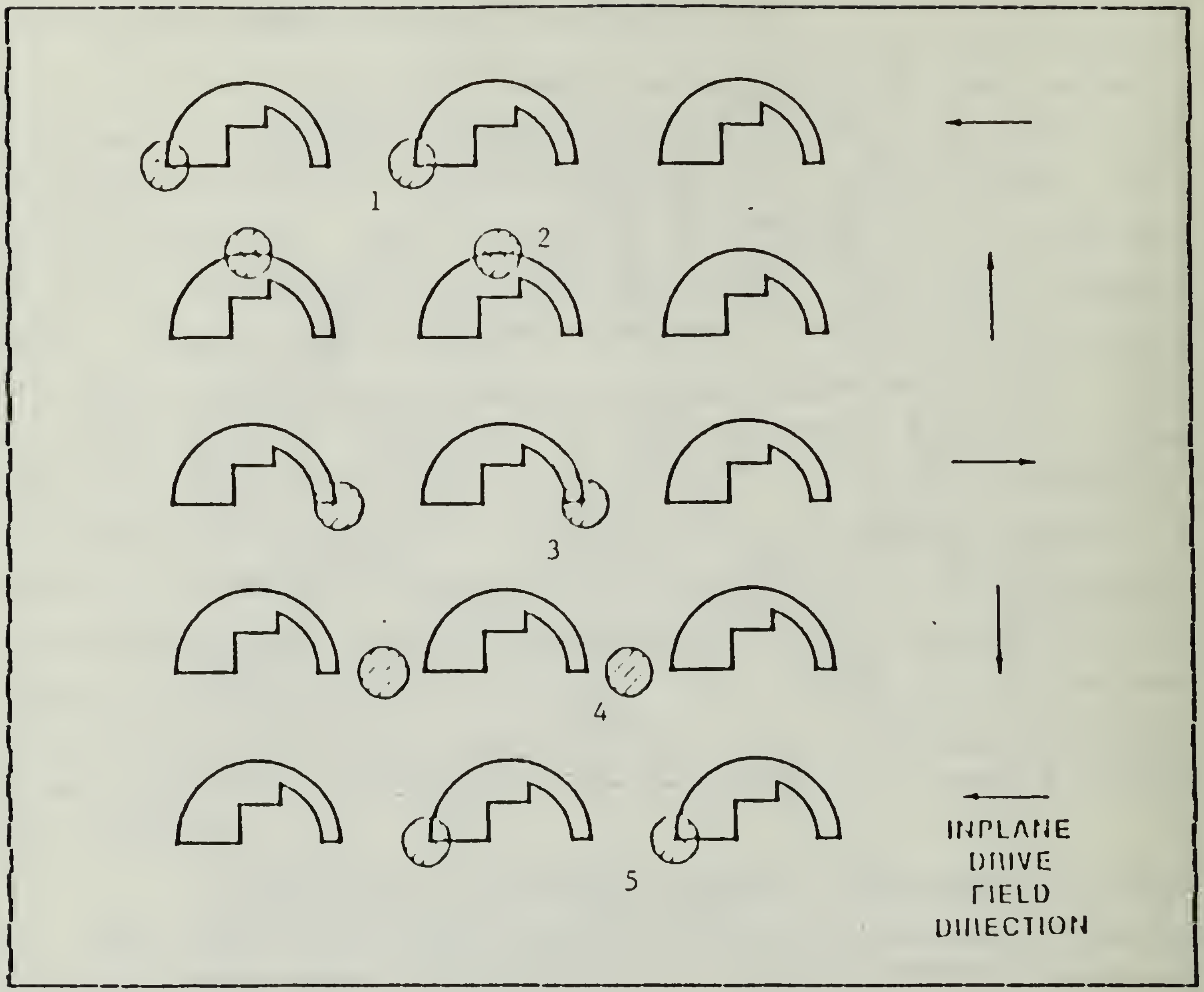


Figure A.6 Movement of Bubbles Beneath a Permalloy Structure Due to a Rotating Magnetic Field.

each permalloy chevron to position 2 pulling the stored magnetic bubbles along. Positions 3 and 4 show the bubble positions during subsequent 90 degree shifts of the applied field vector. Finally position 5 shows that after one complete rotation of the applied field the "field well" returns to its original position on the chevron. Bubbles that were at the end of one chevron are drawn across the gap to the "field well" of the next permalloy structure. Bubbles are simply shifted linearly by one location each complete cycle of the rotating magnetic field.

4. Data Storage Organization

Since movement of the magnetic bubbles within the substate is essentially serial between adjacent locations, digital data could be stored by placing the data into one long loop of chevrons a single bit at a time as depicted in Figure A.7. This configuration has two major drawbacks. First, a defect in a single chevron would break the continuity of the storage loop and the entire chip would be useless. Secondly, retrieval of particular data would be potentially slow since the desired data may need to be rotated completely around the storage loop before arriving at the output location.

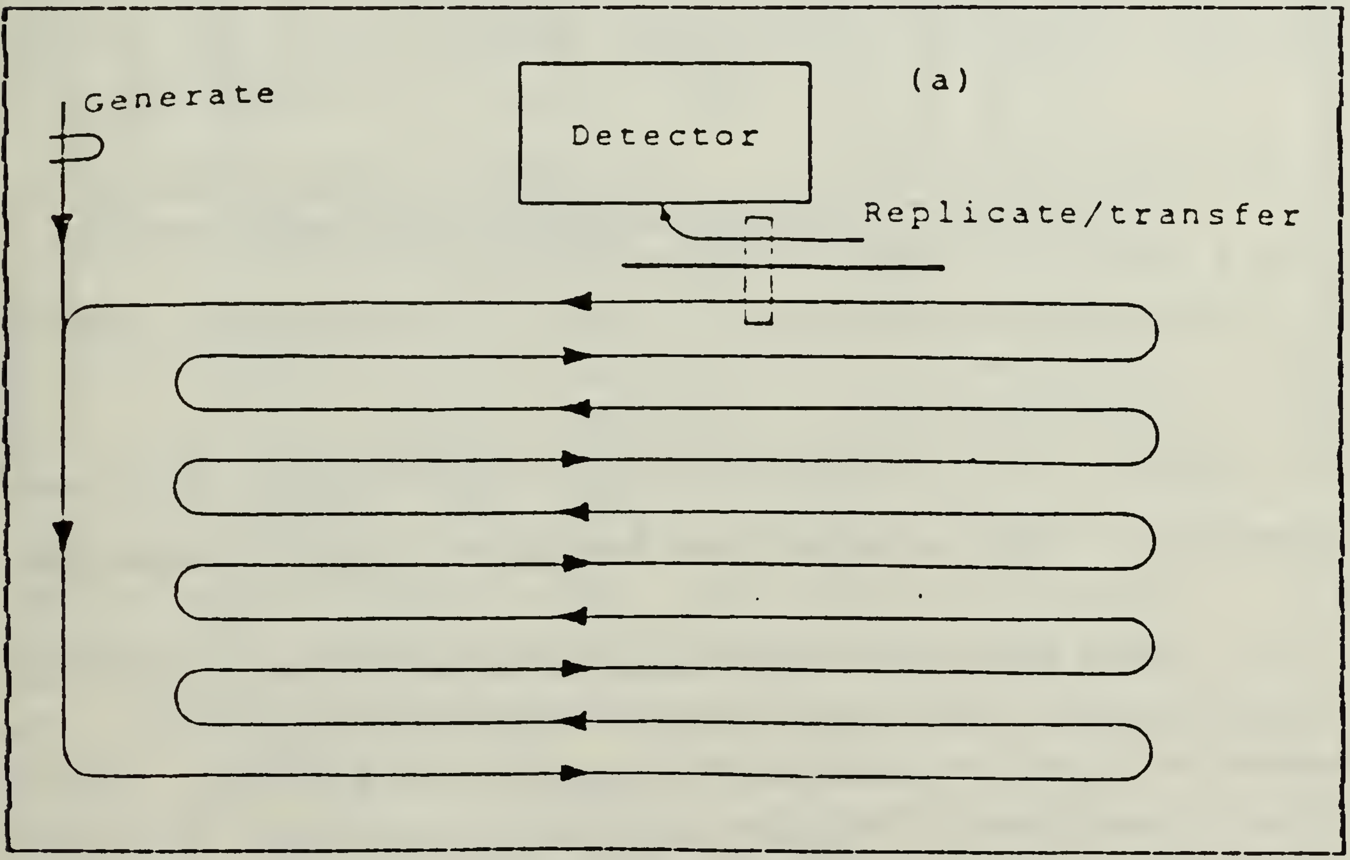


Figure A.7 Single Loop Bubble Storage Architecture.

Figure A.8 shows the most accepted method of storing magnetic bubble data known as the major-track/minor-loop configuration. The major tracks are used for input and output while the minor loops are used for data storage. The method of introducing bubbles for storage and retrieving bubbles as output data is discussed shortly.

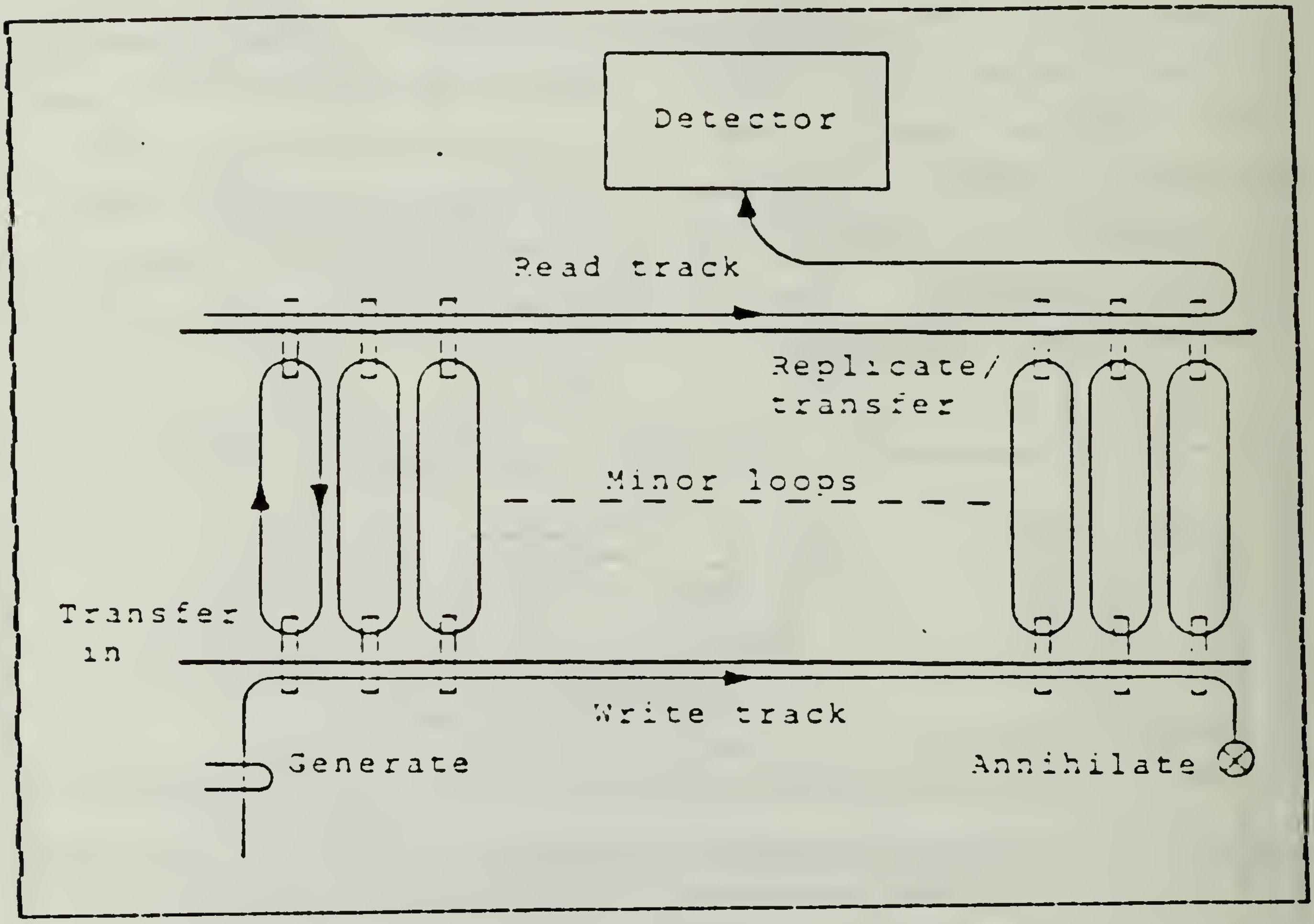


Figure A.8 Major/Minor Loop Bubble Storage Architecture.

Each minor (storage) loop consists of many permalloy chevrons configured in a single continuous path with the input and output locations at opposite end of the loop as shown. Bubbles are passed from the input track to a minor loop and moved from storage location (chevron) to adjacent storage location with each complete circuit of the rotating magnetic field. Stored digital data continuously revolves around the loop while the memory is active, or resides motionless beneath a storage location chevron when the rotating magnetic field is inactive. The major/minor loop configuration makes each data bubble available at most after one rotation of data through one of the smaller minor loops plus the time to move the bubble along the output track. For a fixed number of minor loops with a known number of storage locations per loop, the access time of the system can be determined from the frequency of the rotating magnetic field.

Manufacture of the memory chip can include fabrication of a number of redundant storage loops onto the substrate. This increases the yield of useable devices containing a specified number of operable storage loops. During testing, defective loops can be identified and a "bootloop" code, representing the operational loops for that specific chip, can be used during input and output processes to ignore faulty or untested loops.

5. Data Bubble Production

Presence of a bubble within a magnetic bubble memory is used to represent a "one" in digital data information. Digital "zeros" are represented by the absence of a bubble in a particular memory location. Data delivered to the memory in digital form must be changed into a series of magnetic bubbles suitable for storage. Since magnetic bubbles can only exist within the substrate material, this transformation must physically occur within the memory cell.

One method of bubble production is called nucleation. A current pulse is transmitted into a hairpin shaped conductor beneath a permalloy structure which momentarily creates a region of reversed magnetic potential to that of the bias field. The resulting bubble is sustained by the bias field and is available for propagation after the bubble is stabilized. This process limits the rate of data input due to the current pulse lengths required and time required for the created domain to stabilize.

The accepted method for bubble production within a bubble memory cell is through use of a "seed" bubble as shown in figure A.9. A permanently contained magnetic bubble revolves with the rotating magnetic field within a structure as shown. As the bubble passes over the conductor strip it is elongated and cut by a short current pulse into two bubbles, one which continues to rotate within the seed bubble structure and one which is available for propagation. For the occurance of a "zero" bit, the bubble is simply not split.

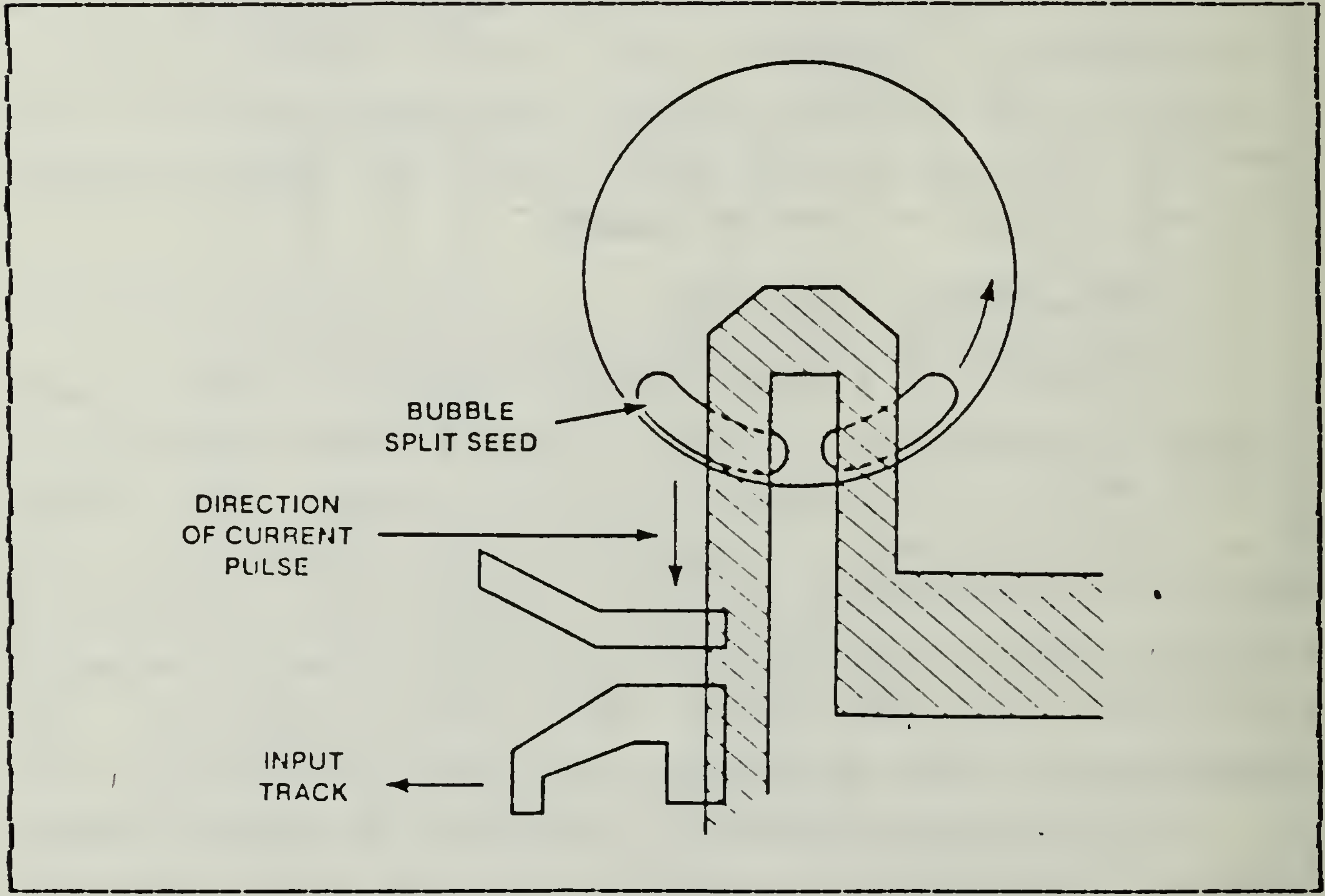


Figure A.9 Bubble Generation for Input.

6. Data Input

As described earlier, the major tracks in the major-track/minor-loop storage architecture represent the paths that magnetic bubbles follow when reading information in to or out of the substrate. Figures A.8 and A.9 show the bubble generator positioned at the beginning of the input track. During an input operation the seed bubble is either split or not split to produce a digital "one" or "zero" for storage. Bubbles created are immediately streamed onto the input track and propagate one location away from the generator each external field rotation making room for the next data bit. As this implies, digital data delivered to the memory must be configured serially for input. Additionally, the data must be arranged in "pages" of streams of bubbles and spaces having the same length as the number of available minor storage loops configured on the substrate. When the data have completely filled the input track, each bit of data is positioned adjacent to a separate storage loop. The entire page is transferred en mass to the minor loops in a single "swap" operation as depicted in Figure A.10. A current pulse is applied through a conductor which causes the bubble in the input track location to move onto the swap gate location at the top of the storage loop and simultaneously moves the bubble previously in the swap gate to the input track location. As a new page of data is streamed onto the input track for storage, the old data bubbles swapped from the storage loops are moved to an area at the end of the input track known as a guard rail where they are annihilated. It is important to note that as the data are rotated about the substrate, data associated with a particular page maintain the same relative positions within the storage loops as all bubbles move simultaneously.

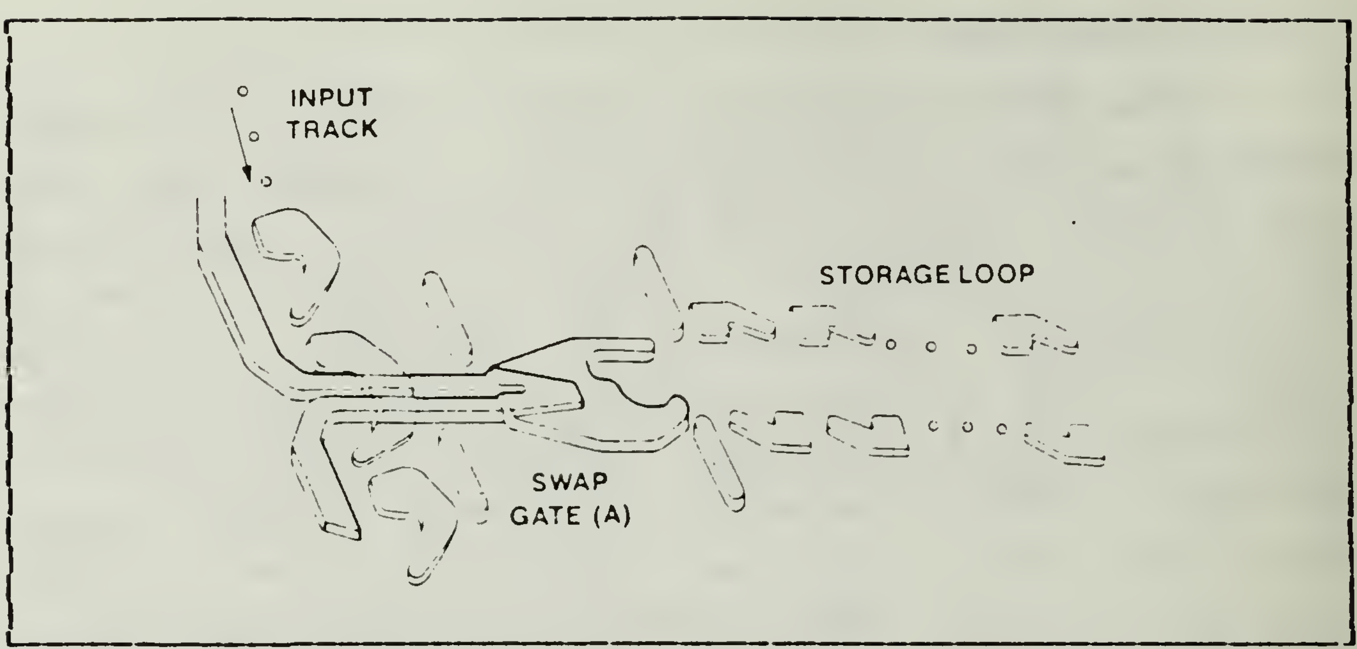


Figure A.10 Input of Data to a Storage Loop.

7. Data Output

At the output side of a minor loop, data to be read are reproduced from the output storage location by a "replicate gate" as depicted in Figure A.11. An applied current pulse stretches and cuts the data bubble in much the same way as in the seed bubble operation, placing the new bubble onto the output track while leaving the original bubble in its storage location. Since the original data remain intact and in original orientation within the memory, the read operation is non-destructive. The replicate operation is conducted simultaneously from all minor loops resulting in retrieval of the page of data in the same serial pattern as established during input of the information.

8. Bubble Detection

The resulting stream of bubbles and spaces representing the read data in page format on the output track is fed serially through a voltage detection circuit which acts on the magneto-resistive effect of its permalloy structure.

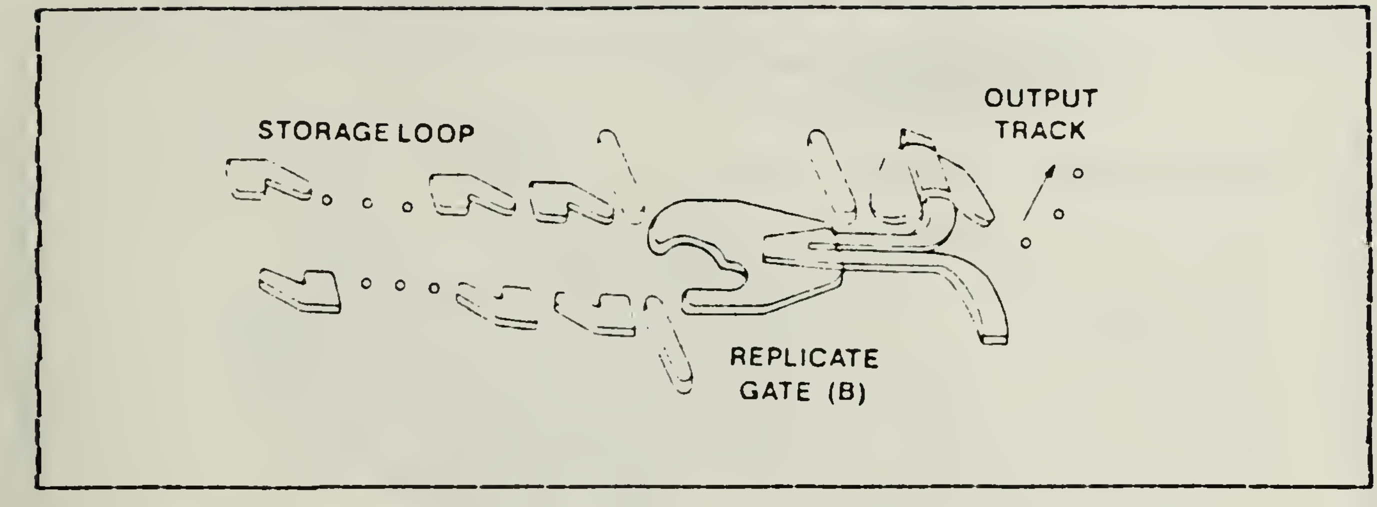


Figure A.11 Output of Data from a Storage Loop.

Presence of a bubble affects the resistivity of the structure as measured by an applied current. The data bubble is first passed through a structure which enlarges the bubble area to increase this effect. The detection circuit is usually paralleled by a dummy detector which provides compensation for resistivity changes attributable to the presence of the rotating magnetic field. Figure A.12 is a representative detection circuit. The microvolt output from the detector representing the stored digital data must be amplified to higher voltage level signals useable by external devices.

9. Data Organization and Addressing

Digital information is arranged in sequences of pages for transfer and remains in page format while stored in a bubble memory system. The dynamic nature of such a system does not retain certain data in any discrete location but does maintain the relative positions between pages by rotating all bubbles around the storage loops simultaneously. External systems utilizing bubble memory must be able to identify specific pages within the memory and retrieve the desired page during a read operation. A

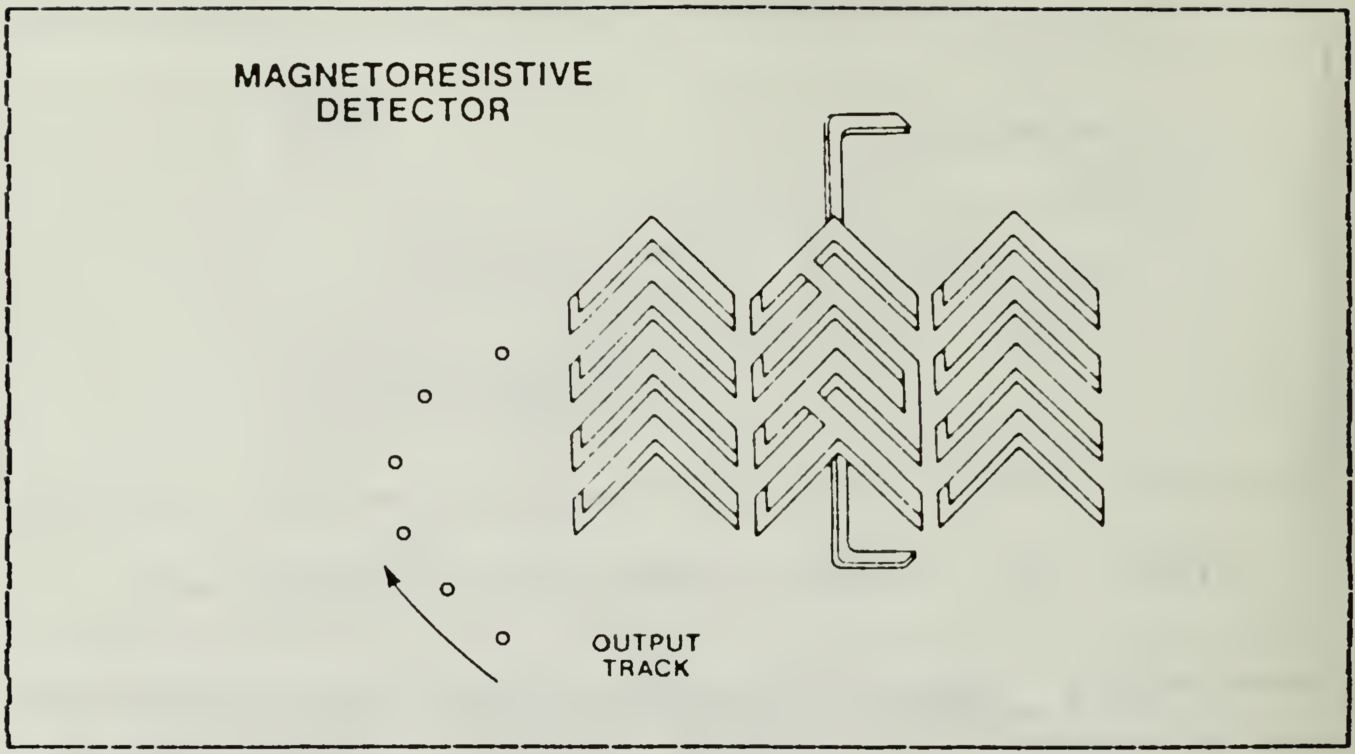


Figure A.12   Magnetic Bubble Detection Circuit.

particular bit of information associated with a particular page stored within the bubble memory cell must be derived from the page after it is retrieved from the system. A header/tail code could facilitate this process if necessary. For use as a digital recorder, the starting and stopping pages for particular information could be stored separately to help identify specific recorded information.

10. Memory Cell Components

The term bubble memory "cell" is used to identify a complete component capable of storing and transferring magnetic bubble digital information. Figure A.13 shows an exploded view of the main components that make up an individual memory cell. The entire package is usually contained within a structure designed to minimize the effects of the magnetic fields of the device on other memory components. This also provides protection of the stored information from external electro-magnetic interference or the radiations which may be encountered in space.

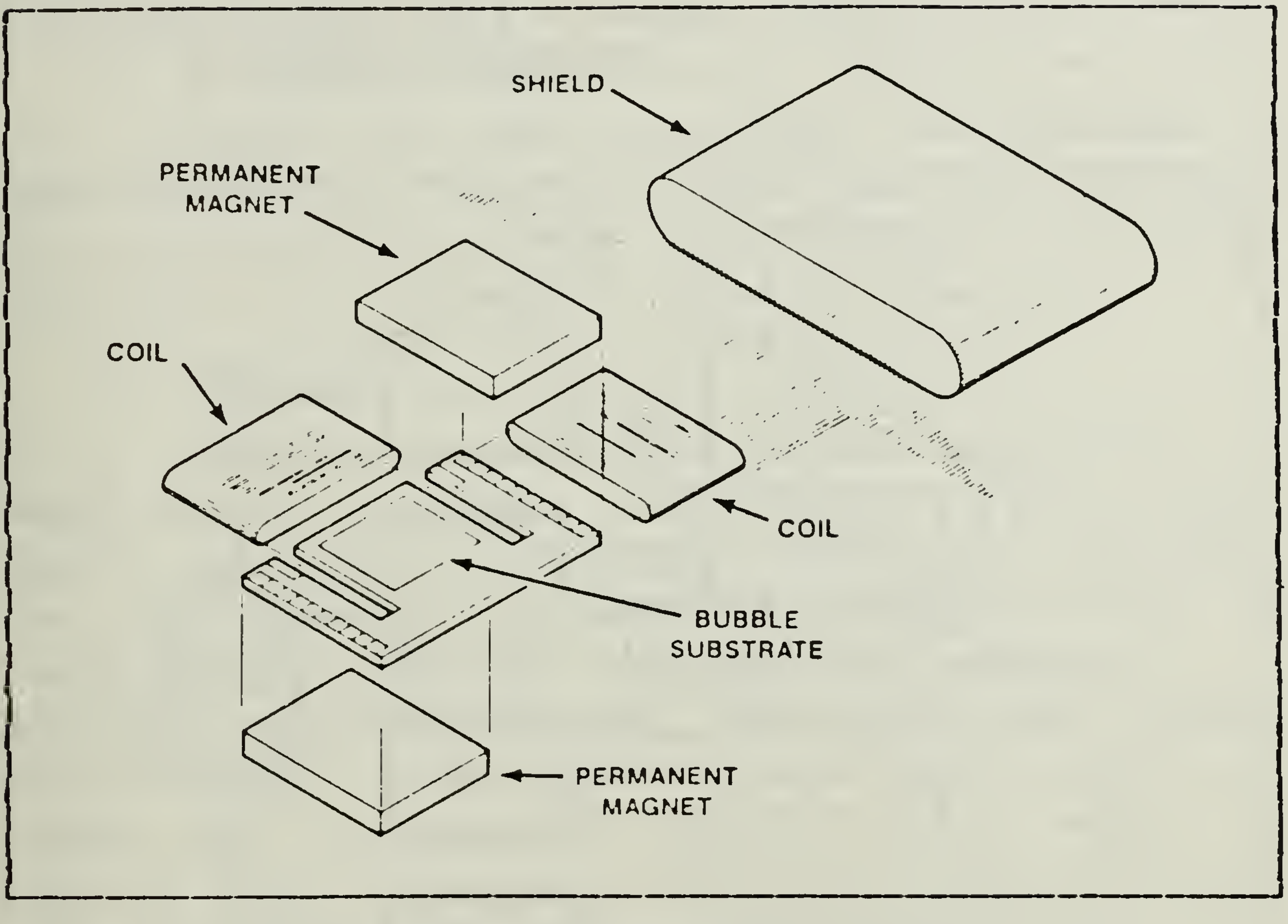


Figure A.13 An Exploded View of a Memory Cell.

B. MEMORY CELL REQUIRED SUPPORT

Figure A.13 describes the main components that make up a memory cell capable of storing and transferring digital information in the form of magnetic bubbles, however this capability requires many of the processes to be initiated and controlled externally. Figure B.10 is a block diagram of a generic magnetic bubble memory system and identifies the major functions provided to a bubble memory for proper operation. Most of these functions were identified in the description of the memory cell and the following subsections address these functions in a general sense as a summary of required memory cell support. Chapter 2 and appendix B present the Intel Corp. components which perform these functions specifically in the Intel-designed system.

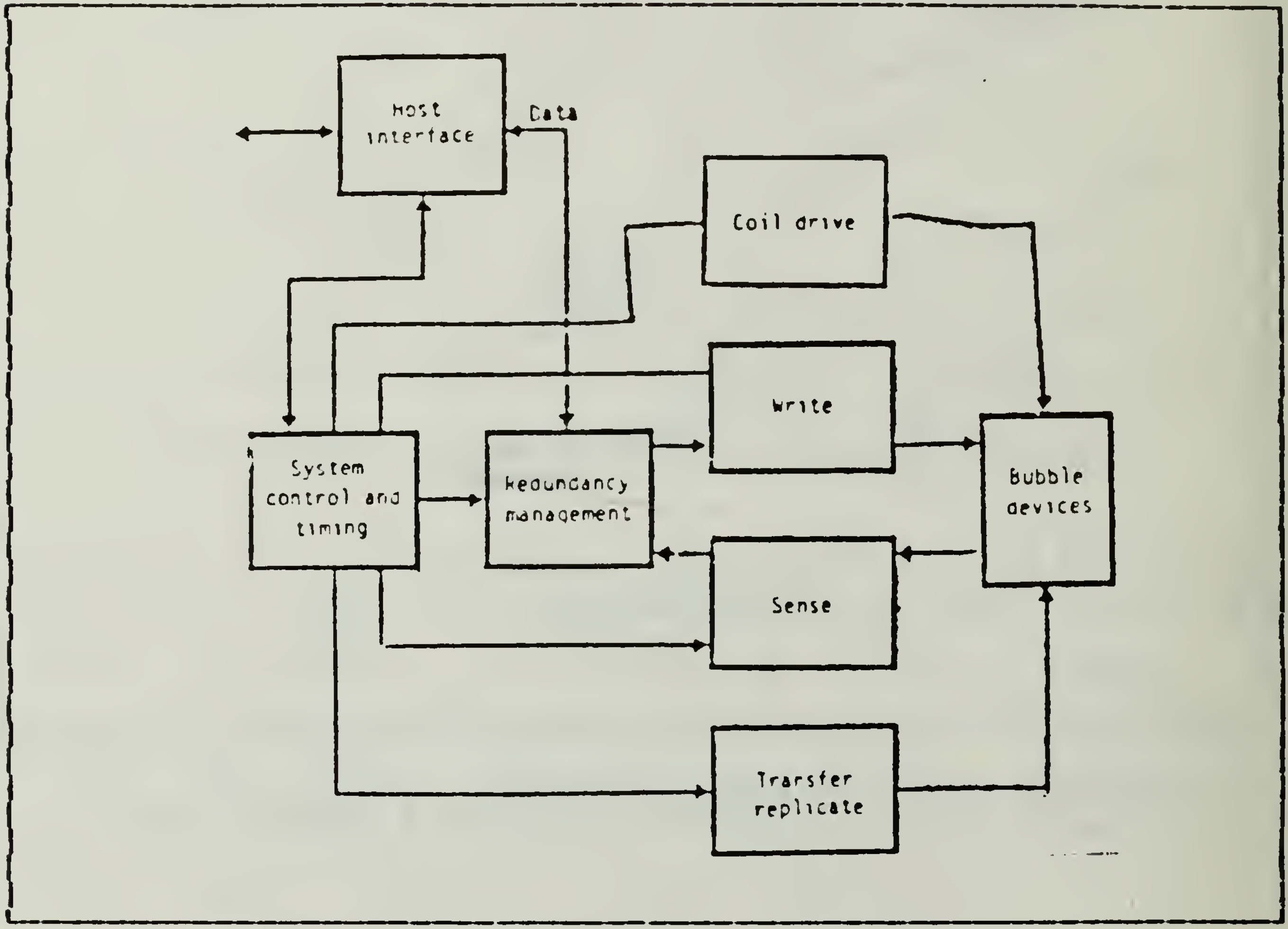


Figure A.14 Magnetic Bubble Memory Required Systems.

1. Current Pulse Production

Current pulses are used by a number of components within the cell. Bubble generation, replication, and swaps require separate current pulses at precise times for proper read and write operations and current pulses to the perpendicular coils control bubble movement within the substrate.

Current must also be provided to the detection circuit in order to measure the magneto-resistive effect of bubble presence during a read.

2. Input/Output Formatter

Digital data must be arranged into sequences of pages for input to the bubble memory. Also, detected microvolt levels must be amplified and rearranged into the original page format for output.

3. Controller

Timing and control of the signals supplied to the memory cell by the support components is the most critical aspect of magnetic bubble memory operation as described. The write operation is a specific example. It must be remembered that whenever the coils are activated, all bubbles within the system move one location each complete field rotation. Bubble generate pulses must be sent at the precise time to arrange the bubbles in proper sequence on the input track. The page of locations in which the information is to be stored must be identified relative to the other storage pages and the locations must arrive at the swap gates at the same instant the bubbles on the input track are aligned with their storage loops. The output process is similar in timing requirements and signal control.

Such a complex system requires a separate controller component to coordinate the operation of the memory cell and its associated support components and to provide an interface to the external system utilizing the magnetic bubble memory.

APPENDIX B

INTEL CORP. MAGNETIC BUBBLE MEMORY COMPONENTS

This appendix describes the Intel Corp. components which are the building blocks used to create the magnetic bubble memory recorder systems described in this paper.

The appendix follows the format of Chapter 2 but presents the components in more detail including chip pin-out signals and internal configurations, if applicable.

This thesis was initially based on the operation and capabilities of components as described in the information available in early 1984. Since then, several anomalies have been identified with the existing system.

Testing of the 7114 MBM chips included identification of enough storage loop pairs to produce the required 8192 to meet design specifications. Pairs of loops were required due to the fact that the bootloop code stored in each half of the memory chip associated one bit with two storage loops. This was necessitated by the limited space available in the FSA bootloop registers. This bootloop coding scheme limited chip production enough to convince Intel to consider re-designing the system to allow a one-for-one coding by increasing the available space within the registers.

An intermediate fix involving additional hardware was developed by Intel and information describing these changes was received early this year. The BPK 5V75A prototype kit systems currently available incorporate an External Added Redundancy Scheme (EARS) to act as an extended bootloop register. An external EPROM, two FSAs, and a significant amount of circuitry are required per bubble memory chip to allow the one-for-one bootloop coding. Need for the additional hardware increases the complexity of the system as well as the size and power consumption, adverse trends for use in space-based systems attempting to minimize these factors.

To resolve the anomalies, Intel Corp. is redesigning two of the existing components and plans release of these chips later this year. Specifically, a new 7225 bubble memory controller chip will replace the 7224 BMC and a new 7245 formmatter/sense amplifier chip will replace the 7244 FSA which will alleviate the need for the additional hardware and offer other benefits as well. These components have been designed to integrate with the remaining original elements of the system and the general descriptions given in Chapter 2 apply equally to both generations of components. However, due to the lack of specific information now available, component descriptions of this appendix do not include the 7225 or 7245 chips. Instead, the existing 7224 BMC and 7244 FSA chips are described and differences expected from use of the new chips mentioned. It must be pointed out that the hardware interfaces associated with the new chips may be slightly different than the existing components. System schematics within this paper are based on the existing chips and may require modification when the new chips are introduced. However, the signals provided to the remaining system elements must be the same as with use of the old chips so the change may turn out to be internal in nature and transparent to the system designer.

A. THE 7114 MAGNETIC BUBBLE MEMORY CHIP

Figure B.1 identifies the 7114 magnetic bubble memory (MBM) chip pin-outs and associated signals. Table 10 gives a short description of each of the pin-out signals identified in the figure including signal origin or destination.

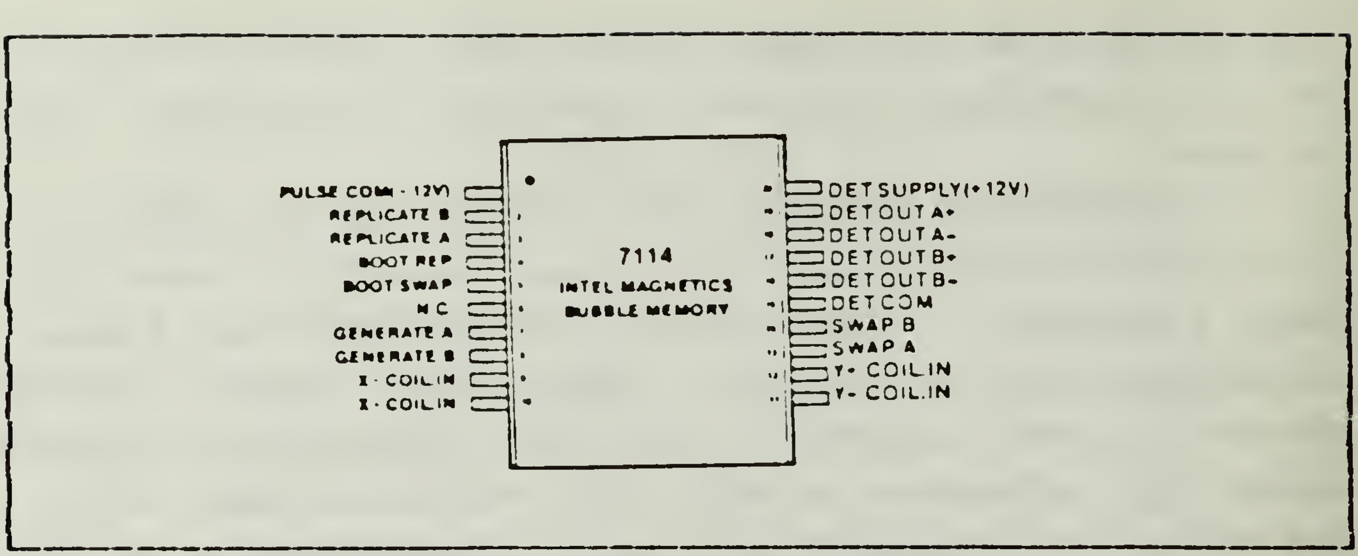


Figure B.1 7114 Magnetic Bubble Memory Chip Schematic.

The 7114 magnetic bubble memory (MBM) chip contains the substrate material in which magnetic bubbles are produced and stored, the permalloy structures which determine bubble location, the permanent magnets which ensure bubble stability, and the perpendicular coils which control bubble movement.

1. Data Storage Configuration

Figure B.2 shows the data storage configuration of one half of the memory cell. Each half system is composed of four "octants" of memory areas with permalloy structures configured in the major-track/minor-loop storage architecture. Each octant has its own seed bubble generator, input track, and output track. Detector circuits are shared by pairs of memory octants.

Each octant has 80 storage loops resulting in 640 total loops per chip. During the manufacturing process each loop is tested and 540 perfectly operating loops are identified. Of these, 512 are used for data storage, 28 are used to hold error correcting codes appended to the information stored within the memory, and 2 contain bootloop information

TABLE 10
7114 MBM Pin-Out Signal Descriptions

Symbol	Pin No	I/O	Source/Destination	Description
BOOT REP	4	I	7234 CPG	Two level current pulse input for reading the boot loop
BOOT SWAP	5	I	7234 CPG	Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM
DET COM	15	I		Ground return for the detector bridge
DET OUT	16 — 19	O	7244 FSA	Differential pair (A+, A−, and B+, B−) outputs which have signals of several millivolts peak amplitude
DET SUPPLY	20	I		+12 volt supply pin
GEN A and GEN B	7, 8	I	7234 CPG	Two level current pulses for writing data onto the input track
PULSE COM	1	I		+12 volt supply pin
REP A and REP B	3, 2	I	7234 CPG	Two level current pulses for replicating data from storage loops to output track
SWAP A and SWAP B	13, 14	I	7234 CPG	Single level current pulse for swapping data from input track to storage loops
X − COIL IN X + COIL IN	9, 10	I	7264	Terminals for the X or inner coil
Y − COIL IN Y + COIL IN	11, 12	I	7264	Terminals for the Y or outer coil

identifying the useable loops. A single bootloop is used to identify the operating loops within one half-system. The remaining non-identified loops are either defective or not used and are masked by the bootloop code. This redundant-loop manufacturing process increases the yield of useable devices.

Each storage loop is made up of 8192 permalloy structures including the input and output locations. This results in a single-chip user storage capacity of 4,194,304 bits (four megabits) cf digital information.

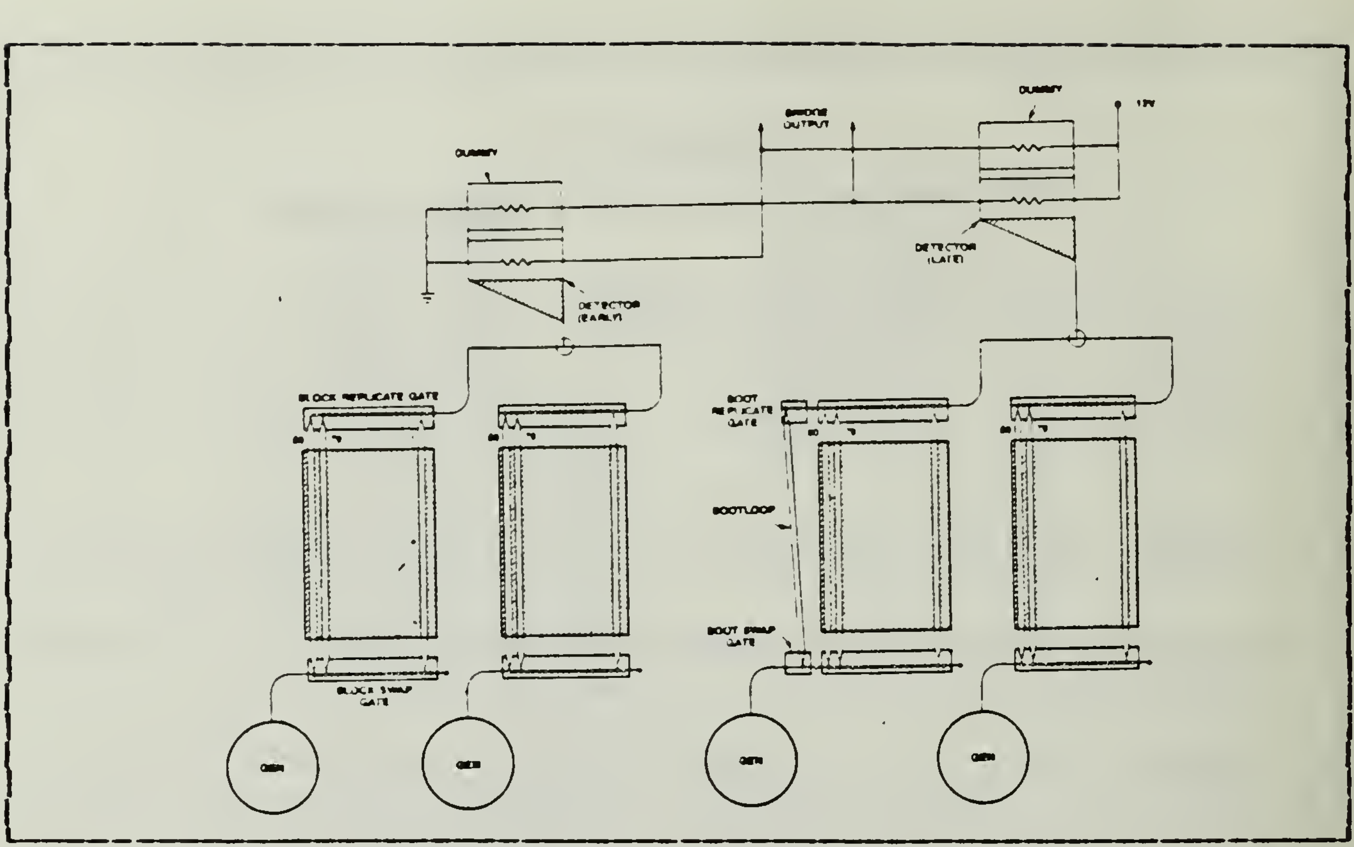


Figure B.2 Intel 7114 Bubble Memory Chip Data Organization.

2. Data Input/Output

In figure B.2 the left two octants are labelled EARLY and the right two labelled LATE. Two bubble generate signals are sent to each half of the memory chip each rotation of the external rotating field, the presence of a binary "one" to be represented by generation of a magnetic bubble for storage with absence of a bubble representing a binary zero. The first signal operates both bubble generators of the EARLY pair of octants creating two identical streams of bubbles and spaces along the input tracks. The second generate signal operates the LATE pair of generators one half rotation of the external field later. Storage loops, and their associated swap gates, are spaced every two propagation locations along the input track. Data on the input track of one of the pairs of octants is delayed by one field rotation placing the odd bits at the swap gates of one octant and the even bits at the swap gates of the other octant within a pair. A single current pulse swap signal operates all swap gates in the memory simultaneously. The duplicated bits on the input tracks not associated with a swap gate, and the old data bits swapped out of the memory and onto the input tracks, propagate to the end of the input tracks as new data is generated. The end of the track is a "rail guard" where these unused bubbles are annihilated.

540 loops are used to store data within the bubble memory chip. 512 hold information sent to the memory for storage, and the remaining loops contain 28 bits of error correcting code appended by an external device to every block of data input for storage. Data must be arranged in 512 bit blocks ("pages") for each input operation and the data streamed onto the input tracks properly to coincide with the desired storage loop locations.

The output process is performed similarly. When the desired data page is rotated under the replicate gate locations, a signal to the memory chip simultaneously reproduces the data onto the output tracks of all the octants. Storage loops are spaced every other location along the output track, so the data of each pair of octants is merged together to before being delivered to the shared detector circuit. The magneto-resistive detector circuit voltage signal is sensed by an external device which reconstructs the original serial configuration of the data.

3. Bootloop

Each half system in the memory chip contains a storage loop dedicated to preserving the information which identifies the operating storage loops in that half system, and synchronization data used to determine the relative position of the pages of stored information. This data is loaded into the dedicated loop after the 540 operating loops are identified during the manufacturing process. The information is used by the support components in configuring the data correctly for input and reading the data correctly during output as well as keeping track of the rotating data pages.

B. THE INTEL 7250 COIL PRE-DRIVER CHIP AND 7264 COIL DRIVE TRANSISTORS

Using timing signals from the bubble memory controller, the 7250 coil pre-driver (CPD) chip produces high current outputs to the 7264 coil drive transistors (CDT) to form the triangular waveforms which drive the perpendicular coils around the 7114 MBM and establish the rotating magnetic field for magnetic bubble movement within the cell.

1. 7250 Coil Pre-Driver

Figure B.3 identifies the 7250 coil pre-driver (CPD) chip pin-outs and associated signals. Table 11 gives a short description of each of the pin-out signals identified in the figure including signal origin or destination.

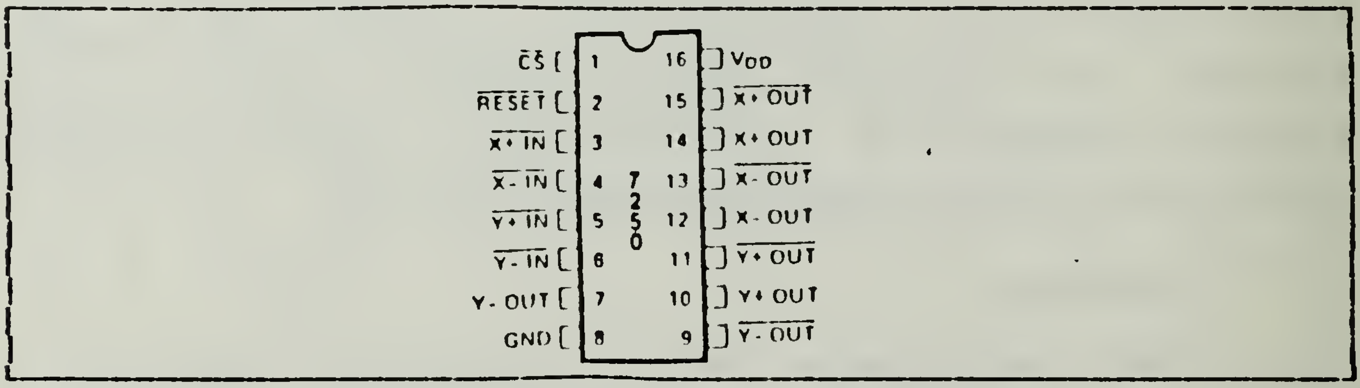
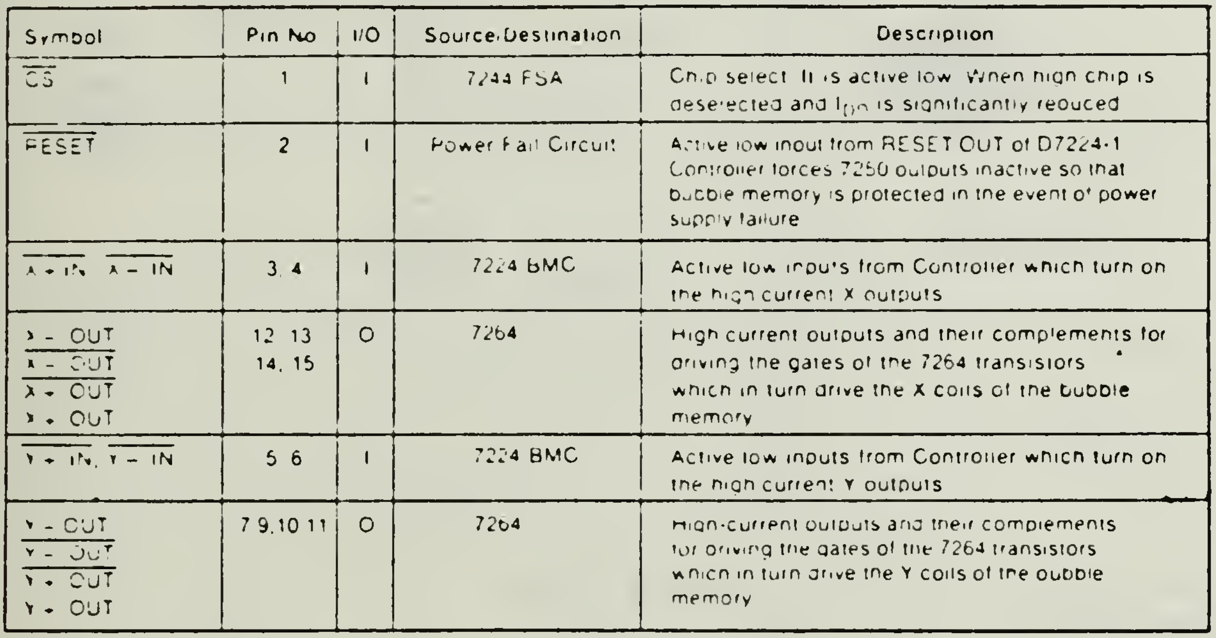


Figure B.3 7250 Coil Pre-Driver Chip Schematic.

TABLE 11
7250 CPD Pin-Out Signal Descriptions



Symbol	Pin No	I/O	Source/Destination	Description
$\overline{CS}$	1	I	7244 FSA	Chip select. It is active low. When high chip is deselected and I_{DD} is significantly reduced
$\overline{RESET}$	2	I	Power Fail Circuit	Active low input from RESET OUT of D7224-1 Controller forces 7250 outputs inactive so that bubble memory is protected in the event of power supply failure
$\overline{X+IN}$, $\overline{X-IN}$	3, 4	I	7224 BMC	Active low inputs from Controller which turn on the high current X outputs
X− OUT $\overline{X-OUT}$ $\overline{X+OUT}$ X+ OUT	12, 13 14, 15	O	7264	High current outputs and their complements for driving the gates of the 7264 transistors which in turn drive the X coils of the bubble memory
$\overline{Y+IN}$, $\overline{Y-IN}$	5, 6	I	7224 BMC	Active low inputs from Controller which turn on the high current Y outputs
Y− OUT $\overline{Y-OUT}$ $\overline{Y+OUT}$ Y+ OUT	7, 9, 10, 11	O	7264	High-current outputs and their complements for driving the gates of the 7264 transistors which in turn drive the Y coils of the bubble memory

2. 7264 Coil Drive Transistors

Figure B.4 depicts the configuration of one set of four matched 7264 coil drive transistors (CDTs) and the associated signals. Two such sets of transistors are required to drive both of the perpendicular coils which surround the substrate material within the 7114 MBM. Table 12 gives a short description of each of the signals identified in the figure including origin and destination.

C. THE INTEL 7234 CURRENT PULSE GENERATOR CHIP

Figure B.5 identifies the 7234 current pulse generator (CPG) chip pin-outs and associated signals. Table 13 gives a short description of each of the pin-out signals identified in the figure including signal origin or destination.

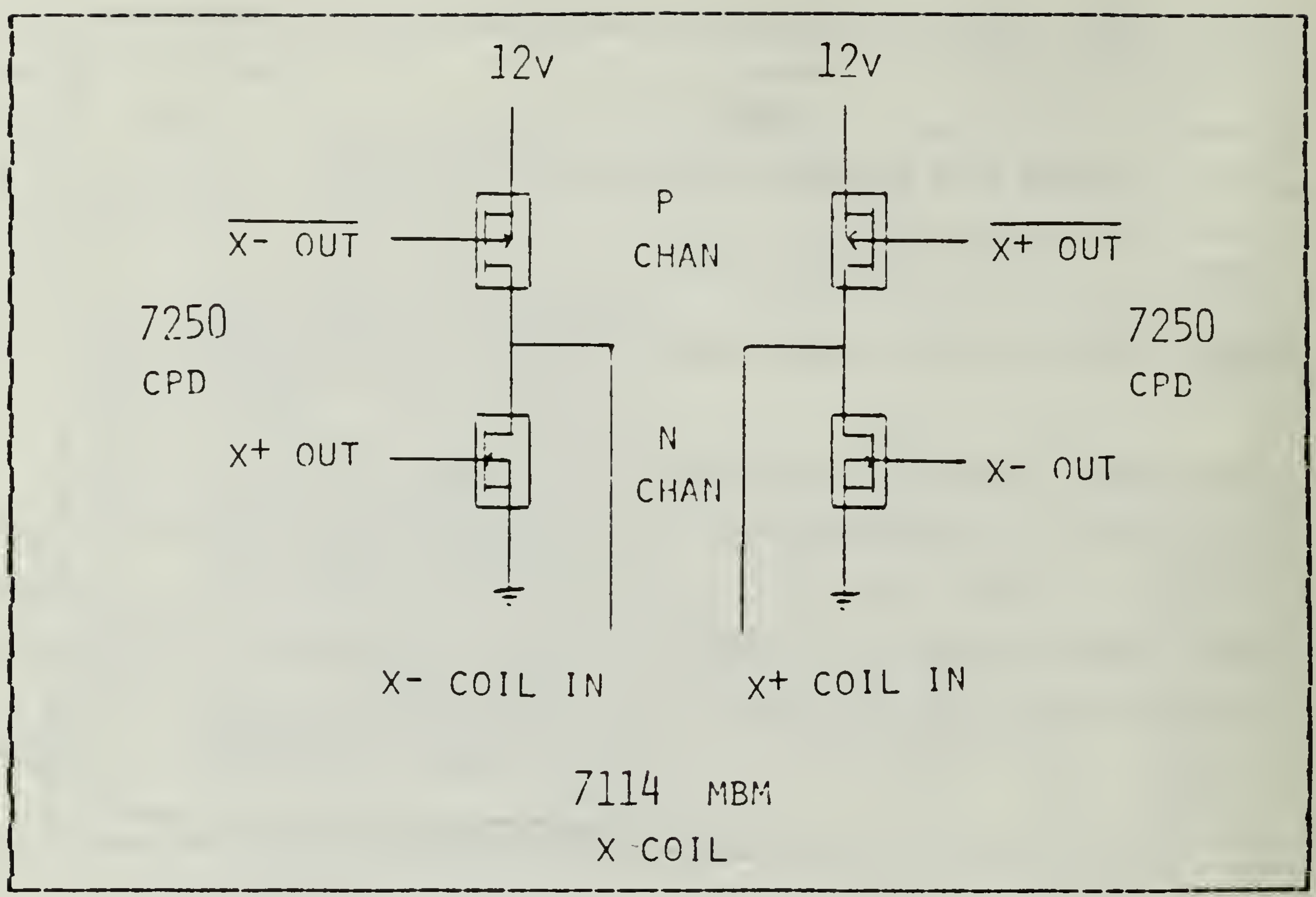


Figure B.4 7264 Coil Drive Transistor Schematic.

Using timing signals from the bubble memory controller and generate signals from the formatting device, the 7234 current pulse generator (CPG) sends current pulse signals to the 7114 MBM which perform the generate, swap, replicate, and bootloop functions during read and write to the memory. The 7234 also monitors both the 12 volt and 5 volt d.c. supplies to the system and produces a power-fail signal to the memory controller if either supply exceeds its threshold values.

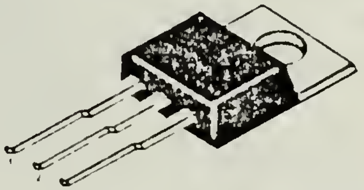
D. THE INTEL 7244 FORMATTER/SENSE AMPLIFIER CHIP

Figure B.6 identifies the 7244 formatter/sense amplifier (FSA) chip pin-outs and associated signals. Table 14 gives a short description of each of the pin-out signals identified in the figure including origin or destination.

TABLE 12
7264 CDT Pin-Out Signal Descriptions

7264

Four matched pair of N- and P-channel transistors In industry standard TO-220 Discrete packaging.


PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

Symbol	Pin No	I/O	Source/Destination	Description
N-Channel				
G	1	I	7250	Gate Drive Signal
D	2	O	7114	Coil Drive Current
S	3	I	Ground	—
P Channel				
G	1	I	7250	Gate Drive Signal
D	2	O	7114	Coil Drive Current
S	3	I	Ground	—

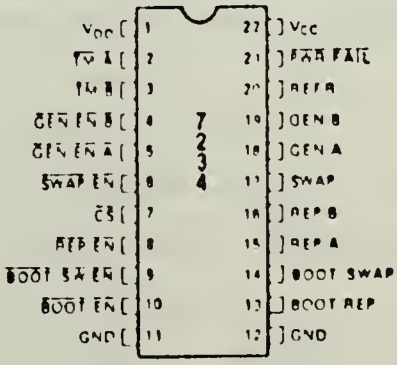
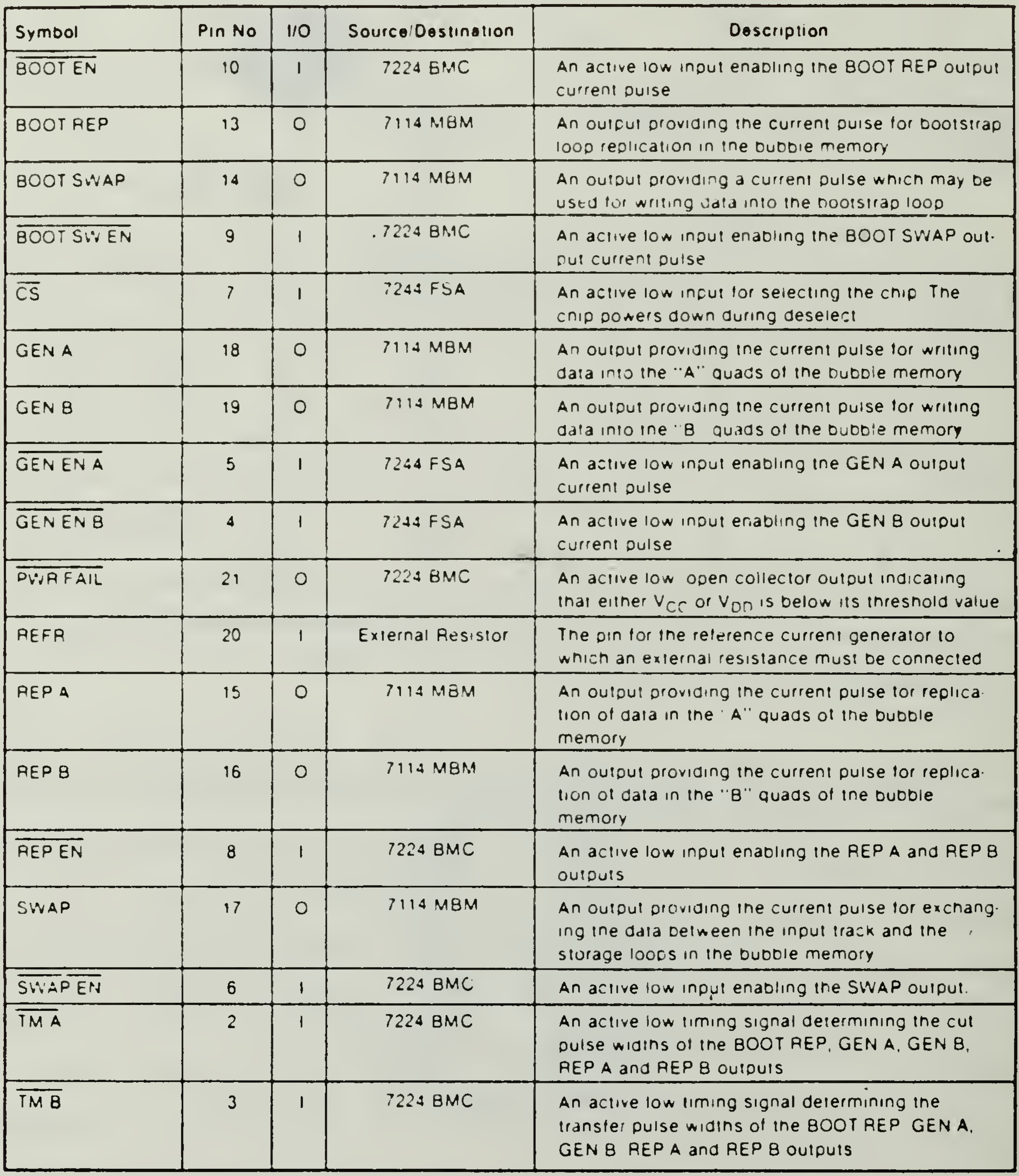


Figure B.5 7234 Current Pulse Generator Chip Schematic.

As the name implies, the 7244 formatter/sense amplifier performs a number of functions concerned in the data transfer within the system. Figure B.7 shows a block diagram of the internal configuration of the device.

TABLE 13

7234 CPG Pin-Out Signal Descriptions



Symbol	Pin No	I/O	Source/Destination	Description
$\overline{\text{BOOT EN}}$	10	I	7224 BMC	An active low input enabling the BOOT REP output current pulse
BOOT REP	13	O	7114 MBM	An output providing the current pulse for bootstrap loop replication in the bubble memory
BOOT SWAP	14	O	7114 MBM	An output providing a current pulse which may be used for writing data into the bootstrap loop
$\overline{\text{BOOT SW EN}}$	9	I	7224 BMC	An active low input enabling the BOOT SWAP output current pulse
$\overline{\text{CS}}$	7	I	7244 FSA	An active low input for selecting the chip The chip powers down during deselect
GEN A	18	O	7114 MBM	An output providing the current pulse for writing data into the "A" quads of the bubble memory
GEN B	19	O	7114 MBM	An output providing the current pulse for writing data into the "B" quads of the bubble memory
$\overline{\text{GEN EN A}}$	5	I	7244 FSA	An active low input enabling the GEN A output current pulse
$\overline{\text{GEN EN B}}$	4	I	7244 FSA	An active low input enabling the GEN B output current pulse
$\overline{\text{PWR FAIL}}$	21	O	7224 BMC	An active low open collector output indicating that either V_{CC} or V_{DD} is below its threshold value
REFR	20	I	External Resistor	The pin for the reference current generator to which an external resistance must be connected
REP A	15	O	7114 MBM	An output providing the current pulse for replication of data in the "A" quads of the bubble memory
REP B	16	O	7114 MBM	An output providing the current pulse for replication of data in the "B" quads of the bubble memory
$\overline{\text{REP EN}}$	8	I	7224 BMC	An active low input enabling the REP A and REP B outputs
SWAP	17	O	7114 MBM	An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory
$\overline{\text{SWAP EN}}$	6	I	7224 BMC	An active low input enabling the SWAP output.
$\overline{\text{TM A}}$	2	I	7224 BMC	An active low timing signal determining the cut pulse widths of the BOOT REP, GEN A, GEN B, REP A and REP B outputs
$\overline{\text{TM B}}$	3	I	7224 BMC	An active low timing signal determining the transfer pulse widths of the BOOT REP GEN A, GEN B REP A and REP B outputs

The FSA is a dual-channeled device with one channel corresponding to one of the half-systems of four octants in the 7114 MBM storage scheme. The bootloop information is

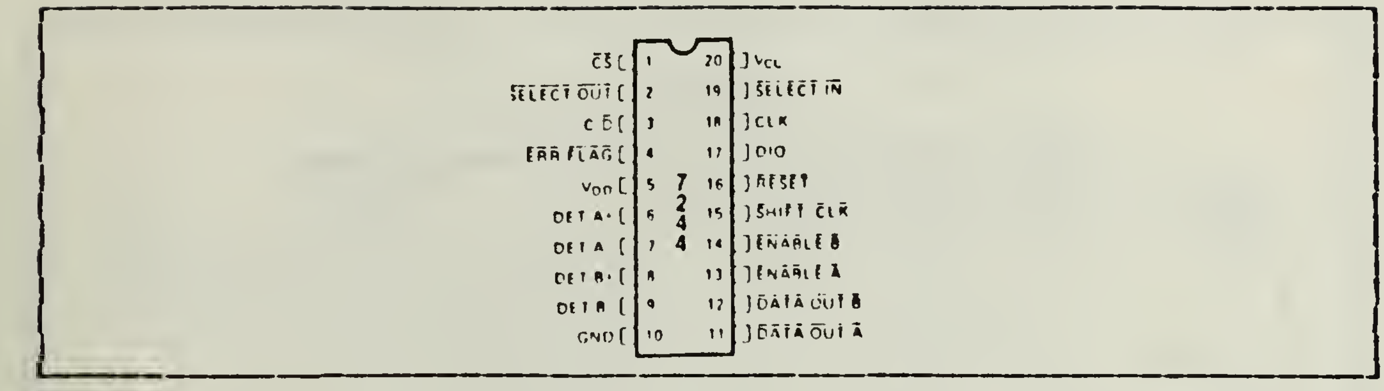

$\overline{CS}$
$\overline{SELECT}$ $\overline{OUT}$
C $\overline{D}$
$\overline{ERR}$ $\overline{FLAG}$
V_{DD}
DET A+
DET A
DET B+
DET B
GND
1
2
3
4
5
6
7
8
9
10
7244
20
19
18
17
16
15
14
13
12
11
V_{CC}
$\overline{SELECT}$ $\overline{IN}$
CLK
DIO
RESET
$\overline{SHIFT}$ $\overline{CLK}$
$\overline{ENABLE}$ $\overline{B}$
$\overline{ENABLE}$ $\overline{A}$
$\overline{DATA}$ $\overline{OUT}$ $\overline{B}$
$\overline{DATA}$ $\overline{OUT}$ $\overline{A}$

Figure B.6 7244 Formatter/Sense Amp Chip Schematic.

stored in a bootloop register to identify the operating loops within the corresponding half-system. Each channel also has a first-in/first-out (FIFO) register used in data transfer to and from the bubble memory. Each FIFO holds 270 bits of which 256 represent half of the 512 data bits per page required for each transfer process. The remaining FIFO spaces hold a 14-bit error correction code appended by the FSA to each 256 bits of data input for storage to the respective half-system.

The FSA also contains an internal status register which is used to communicate the status of the FSA FIFO or information concerning error correction capabilities or types of detected errors.

The serial communications block serves as the interface to the bubble memory controller. The DIO line is a bi-directional serial bus which transfers data and commands between the FSA and the controller. These functions are differentiated by the signal level of the command/data (C/D) line from the bubble memory controller. Commands are sent to the FSA from the controller as one of the four bit words described in table 15. These commands are sent to the FSA automatically by the bubble memory controller to conduct the operation requested by the external system. No direct interaction is required by the external system in sending the FSA

TABLE 14

7244 FSA Pin-Out Signal Descriptions

Symbol	Pin No.	I/O	Source/Destination	Description
$C/\overline{D}$	3	I	7224 BMC	Command/$\overline{\text{Data}}$ signal This signal shall cause the FSA to enter a receive command mode when high and to interpret the serial data line as data when low Any previously active command will be immediately terminated by $C/\overline{D}$
CLK	18	I	Clock	Same TTL level clock used to generate internal timing as used for D7224-1
$\overline{CS}$	1	I	External	An active low signal used for multiplexing of FSAs The FSA is disabled whenever $\overline{CS}$ is high (i e it presents a high impedance to the bus and ignores all bus activity)
$\overline{\text{DATA OUT A}}$ $\overline{\text{DATA OUT B}}$	11, 12	O	7234 CPG	Output data from the FIFO to the MBM generate circuitry Used to write data into the bubble device (active low)
DET A+, DET A− DET B+, DET B−	6, 7, 8, 9	I	7114 MBM	Differential signal lines from the MBM detector
DIO	17	I/O	7224 BMC	The Serial Bus data line (a bidirectional active high signal)
$\overline{\text{ENABLE A}}$ $\overline{\text{ENABLE B}}$	13, 14	O	7234 CPG/7250	TTL level outputs utilized as chip selects for other interface circuits They shall be set and reset by the Command Decoder under instruction of the Controller (active low)
$\overline{\text{ERR FLG}}$	4	O	7224 BMC	An error flag used to interrupt the Controller to indicate that an error condition exists It shall be an open drain active low signal
$\overline{\text{RESET}}$	16	I	Power Fail Circuit	An active low signal that shall reset all flags and pointers in the FSA as well as disabling the chip as the CS signal does The $\overline{\text{RESET}}$ pulse width must be 5 clock periods to assure the FSA is properly reset
$\overline{\text{SELECT IN}}$	19	I	7224 BMC	An input utilized for time division multiplexing An active low signal whose presence indicates that the FSA is to send or receive data from the Serial Bus during the next two clock periods
$\overline{\text{SELECT OUT}}$	2	O	7244 FSA	The $\overline{\text{SELECT IN}}$ pulse delayed by two clocks It shall be connected to the $\overline{\text{SELECT IN}}$ pin of the next FSA It is delayed by two clocks because the FSA is a dual channel device Channel A shall internally pass $\overline{\text{SELECT IN}}$ to Channel B (delayed by one clock)
$\overline{\text{SHIFT CLK}}$	15	I	7224 BMC	A Controller generated clock signal that shall be used to clock data out of the bubble I/O Output Latch to the bubble module during a write operation and to cause bubble signals to be converted by the Sense Amp and clocked into the Bubble I/O Input Latch on a read

command codes or any other of the bubble memory operating control signals.

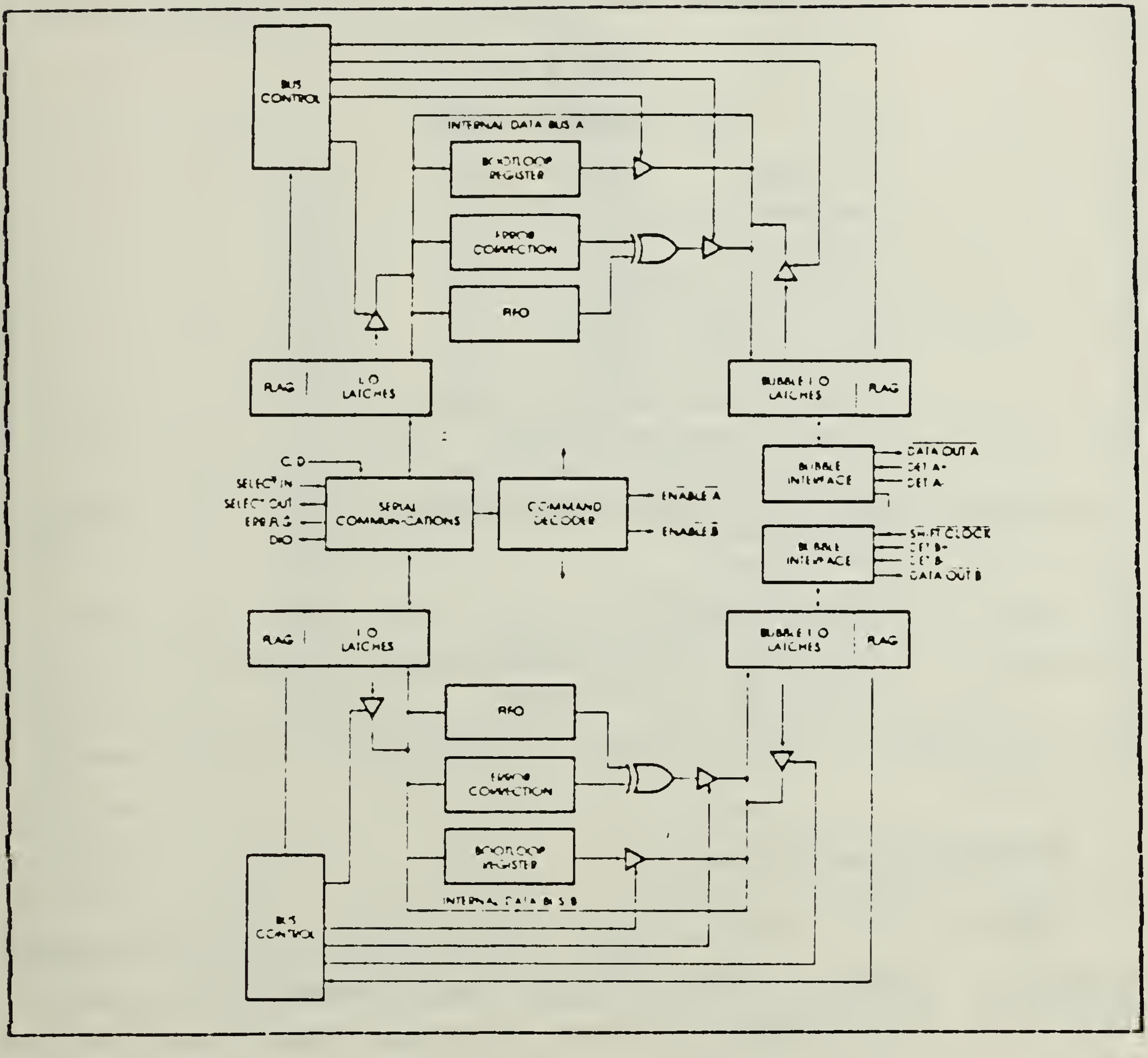


Figure B.7 7244 Formatter/Sense Amp Internal Block Diagram.

E. THE FOUR-MEGABIT MEMORY MODULE

The components described above are combined to form a magnetic bubble memory "module" capable of storing up to four-megabits of digital information. This module represents the smallest building block component on which designs of larger capacities and capabilities may be built.

TABLE 15

FSA Command Codes

NAME	CODE
No Operation	0000
Reserved	0001
Software Reset	0010
Initialize	0011
Write MBM Data	0100
Read MBM Data	0101
Internally Corrected Data	0110
Read Corrected Data	0111
Write Bootloop Register	1000
Read Bootloop Register	1001
Reserved	1010
Reserved	1011
Set Enable Bit	1100
Read ERR.FLG/ Status	1101
Set Correction Enable Bit	1110
Read Status Register	1111

F. THE 7224 CONTROLLER

Figure B.8 identifies the 7224 magnetic bubble memory controller (BMC) chip pin-outs and associated signals. Tables 16 and 17 give a short description of each of the pin-out signals identified in the figure including signal origin or destination.

The 7224 controller is designed to coordinate the efforts of the support components for proper operation of the 7114 MBM chip. The controller provides the support chips with the timing signals critical for controlled movement of the bubbles within the chip, proper creation and sequencing of bubbles for input, and for timely production of swap and replicate signals as required for data input and output from the memory storage loops.

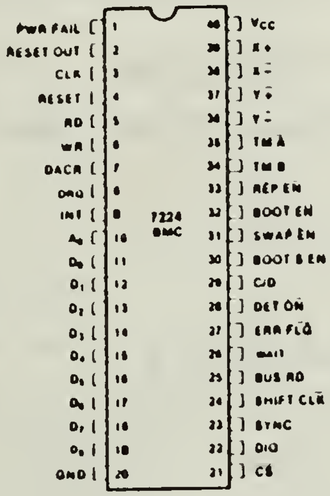


Figure B.8 7224 Bubble Memory Controller Chip Schematic.

The controller also serves as the interface between the memory system and external systems utilizing the memory. Based on commands received from the external system, the bubble memory controller automatically generates the required signals to the support components to conduct the requested operation, with no further action required by the external system other than to provide or accept data from the memory system at a known rate.

A single bubble memory controller is designed to control up to eight bubble memory chips simultaneously.

1. 7224 BMC Internal Configuration

The internal configuration of the bubble memory controller is as shown in the block diagram of figure B.9. The functions of the individual sections are briefly described.

a. Sequencer

The execution and timing of memory operations is coordinated through the sequencer.

TABLE 16

7224 BMC Pin-Out Signal Descriptions

Signal Name	Pin No	I/O	Source/Destination	Description
V_{CC}	40	I		+5 VDC Supply
GND	20	I		Ground
$\overline{\text{PWR FAIL}}$	1	I	7234 CPG	A low forces a controlled stop sequence and holds BMC in an IDLE state (similar to $\overline{\text{RESET}}$)
$\overline{\text{RESET OUT}}$	2	O	7250 CPD 7244 FSA 7234 Reference Current Switch	An active low signal to disable external logic initiated by $\overline{\text{PWR FAIL}}$ or $\overline{\text{RESET}}$ signals but not active until a stopping point in a field rotation is reached (if the BMC is causing the bubble memory drive field to be rotated)
CLK	3	I	Host Bus	2 MHz TTL level clock
$\overline{\text{RESET}}$	4	I	Host Bus	A low on this pin forces the interruption of any BMC sequencer activity performs a controlled shut-down and initiates a reset sequence After the reset sequence is concluded a low on this pin causes a low on the $\overline{\text{RESET OUT}}$ pin, furthermore, the next BMC sequencer command must be either the Initialize or Abort command, all other commands are ignored
$\overline{\text{RD}}$	5	I	Host Bus	A low on this pin enables the BMC output data to be transferred to the host data bus (D_0-D_8)
$\overline{\text{WR}}$	6	I	Host Bus	A low on this pin enables the contents of the host data bus (D_0-D_8) to be transferred to the BMC.
$\overline{\text{DACK}}$	7	I	Host Bus	A low signal is a DMA acknowledge This notifies the BMC that the next memory cycle is available to transfer data This line should be active only when DMA transfer is desired and the DMA ENABLE bit has been set $\overline{\text{CS}}$ should not be active during DMA transfers except to read status If DMA is not used, $\overline{\text{DACK}}$ requires an external pullup to V_{CC} (5 1K ohm)
DRQ	8	O	Host Bus	A high on this pin indicates that a data transfer between the BMC and the host memory is being requested
INT	9	O	Host Bus	A rising edge on this pin indicates that the BMC has a new status and requires servicing when enabled by the host CPU
A_0	10	I	Host Bus	A high on this pin selects the command/status registers A low on this pin selects the data register
D_0-D_7	11-18	I/O	Host Bus	Host CPU data bus An eight-bit bidirectional port which can be read or written by using the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes D_0 shall be the LSB
D_8	19	I/O	Host Bus	Parity bit

b. System Bus Interface

The system bus interface allows the bubble memory controller to interact with an external system to ensure transference of data to and from the memory system at the rate which is set by the number of memory modules being accessed simultaneously. The 7224 BMC is capable of sustaining a transfer rate with an external system of up to one-megabyte per second which is more than adequate for all possible system operating configurations.

c. FSA Select Logic

Timing between the controller and the FSAs is accomplished through this logic. Multi-memory module operation differs significantly from single module operation as was described in Chapter 2.

d. Powerfail, Abort, Reset Logic

To preserve data integrity within the 7114 MBM the system must be shut down in a known manner. In the case of a power failure or a commanded abort/reset, the shut-down routine is activated by this section of the controller.

e. Register File

Six registers are accessed by the external system to prepare the system for the up-coming operations. The registers specify the operation to be conducted, the amount of data to be transferred, the bubble cell to be addressed, and the method to be used in the transfer. A register is also used to report the status of the operation and the occurance of any errors or complications.

Operation of the bubble memory system requires frequent interaction with the BMC registers as was described in Chapter 3.

TABLE 17

7224 BMC Pin-Out Signal Descriptions (cont.)

Signal Name	Pin No.	I/O	Source/Destination	Description
$\overline{\text{CS}}$	21	I	Host Bus	Chip Select Input A high on this pin shall disable the device to all but DMA transfers (i e , it ignores bus activity and goes into a high impedance state)
DIO	22	I O	7244 FSA	A bidirectional active high data line that shall be used for serial communications with 7244 FSA devices
$\overline{\text{SYNC}}$	23	O	7244 FSA	An active low output utilized to create time division multiplexing slots in a 7244 FSA chain It shall also indicate the beginning of a data or command transfer between BMC and 7244 FSA
$\overline{\text{SHIFT CLK}}$	24	O	7244 FSA	A controller generated clock that initiates data transfer between selected FSAs and their corresponding bubble memory devices. The timing of $\overline{\text{SHIFT CLK}}$ shall vary depending upon whether data is being read or written to the bubble memory
$\overline{\text{BUS RD}}$	25	O	To User External Circuit	An active low signal that indicates that the DIO line is in the output mode, i e , BMC is sending data to FSA It shall be used to allow off-board expansion of 7244 FSA devices
$\overline{\text{WAIT}}$	26	I/O	To Alternate Controller(s) When User System Uses More Than One Controller	A bidirectional pin that shall be tied to the WAIT pin on other BMCs when operated in parallel It shall indicate that an interrupt has been generated and that the other BMCs should halt in synchronization with the interrupting BMC $\overline{\text{WAIT}}$ is an open collector active low signal Requires an external pullup resistor to V_c (5 1K ohm)
$\overline{\text{ERR FLG}}$	27	I	7244 FSA	An active low input generated externally by 7244 FSA indicating that an error condition exists It is an open collector input which requires an external pullup resistor (5 1K ohm)
$\overline{\text{DET ON}}$	28	O	To User External Circuit	An active low signal that indicates the system is in the read mode and may be detecting It is useful for power saving in the MBM
$\text{C}/\overline{\text{D}}$	29	O	7244 FSA	A high on this line indicates that the BMC is beginning an FSA command sequence A low on this line indicates that the BMC is beginning a data transmit or receive sequence
$\overline{\text{BOOT SW EN}}$	30	O	7234 CPG	An active low signal which may be used for enabling the BOOT SWAP of the 7234 CPG
$\overline{\text{SWAP EN}}$	31	O	7234 CPG	An active low signal used to create the swap function in external circuits
$\overline{\text{BOOT EN}}$	32	O	7234 CPG	An active low signal enabling the bootstrap loop replicate function in external circuitry
$\overline{\text{REP EN}}$	33	O	7234 CPG	An active low signal used to enable the replicate function in external circuitry
$\overline{\text{TM B}}$	34	O	7234 CPG	An active low timing signal generated by the decoder logic for determining TRANSFER pulse width.
$\overline{\text{TM A}}$	35	O	7234 CPG	An active low timing signal generated by the decoder logic for determining CUT pulse width.
$\overline{\text{Y}-}$, $\overline{\text{Y}+}$, $\overline{\text{X}-}$, $\overline{\text{X}+}$	36-39	O	7250 CPD	Four active low timing signals generated by the decoding logic and used to create coil drive currents in the bubble memory device

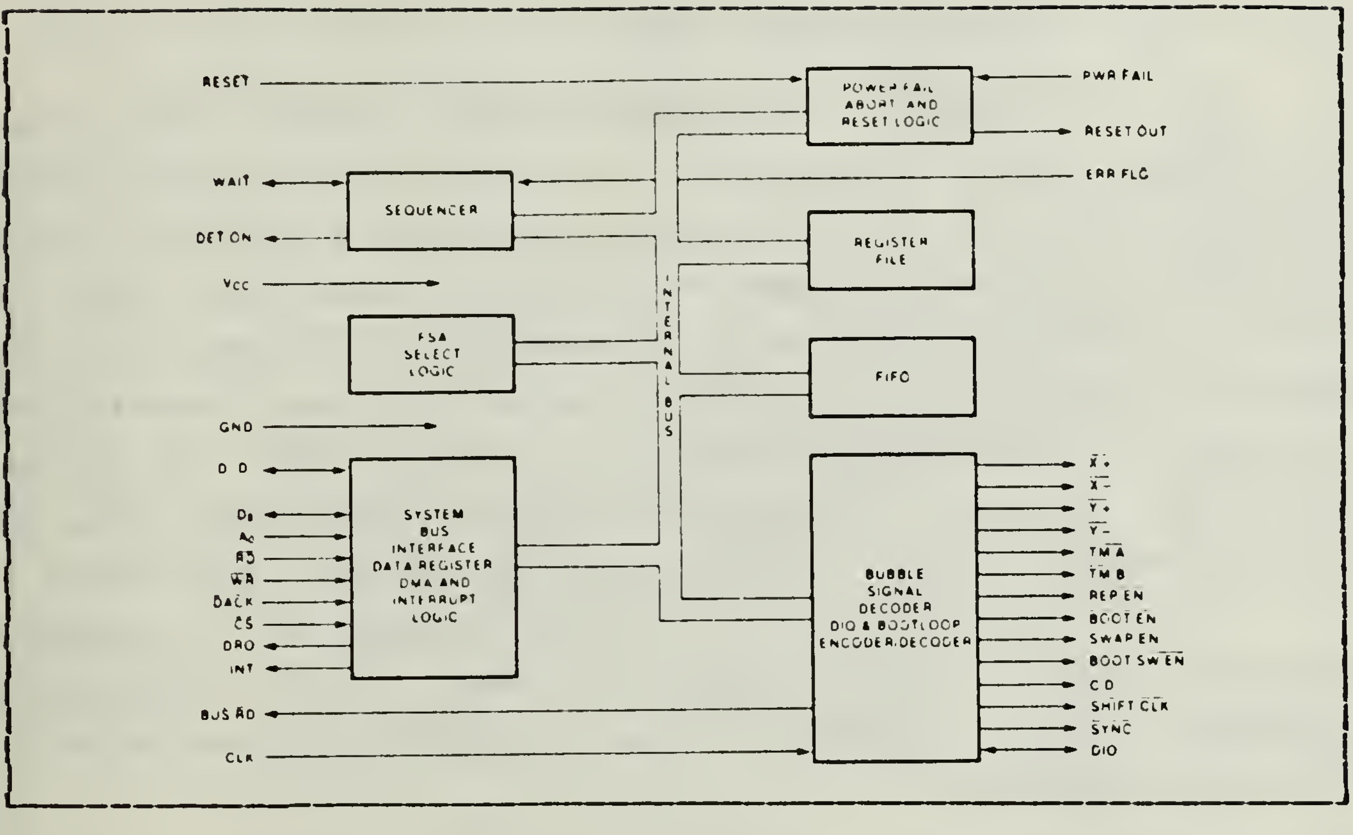


Figure B.9 7224 BMC Internal Configuration Block Diagram.

f. FIFO

The FIFO is a 40 x 8 bit[5] first-in/first-out RAM used as a data buffer between the bubble memory and the external system. Data is transferred between the BMC FIFO and the FSA FIFO at a fixed rate which is multiplied by the number of FSAs within the system. The average data transfer rate to a single memory module is 16 kbytes per second.

---

[5] The FIFO in the 7225 bubble memory controller is to be increased up to 124 x 8 bits. This equates to two full single bubble memory pages. This improvement should make data transfers easier to accomplish and will protect the system from errors due to timing differences between the bubble memory and the external system better than the 7224 BMC.

g. Signal Decoder / DIO

Signals to the bubble memory system must occur at specific times in relation to the rotating magnetic field which corresponds to bubble position within the memory. This functional section of the controller contains the logic to create these timing signals. This section also performs the serial-to-parallel and parallel-to-serial data conversions required to communicate with the 7244 FSA over the serial DIO line. Finally, this section also contains the logic to encode/decode the bootloop information for use by the FSA.

Figure A.14 is a circuit diagram of a complete magnetic bubble memory system composed of the components described above, capable of storing up to four-megabits of digital information.

G. MULTIPLE MODULE SYSTEM CONFIGURATIONS

A single 7224 bubble memory controller is capable of operating up to eight memory modules simultaneously. Figure B.11 shows how the system as depicted in figure B.10 is expanded to incorporate multiple magnetic bubble memory modules.

The benefits of multiple module operations is presented in Chapter 2 and will not be repeated here. However, the method of communication between the bubble memory controller and the multiple FSAs servicing their respective memory modules is discussed in the next subsection.

1. BMC - FSA Communications

Figure B.12 highlights the interconnections between the BMC and multiple FSAs to help explain the method of communication between the bubble memory controller and multiple memory modules.

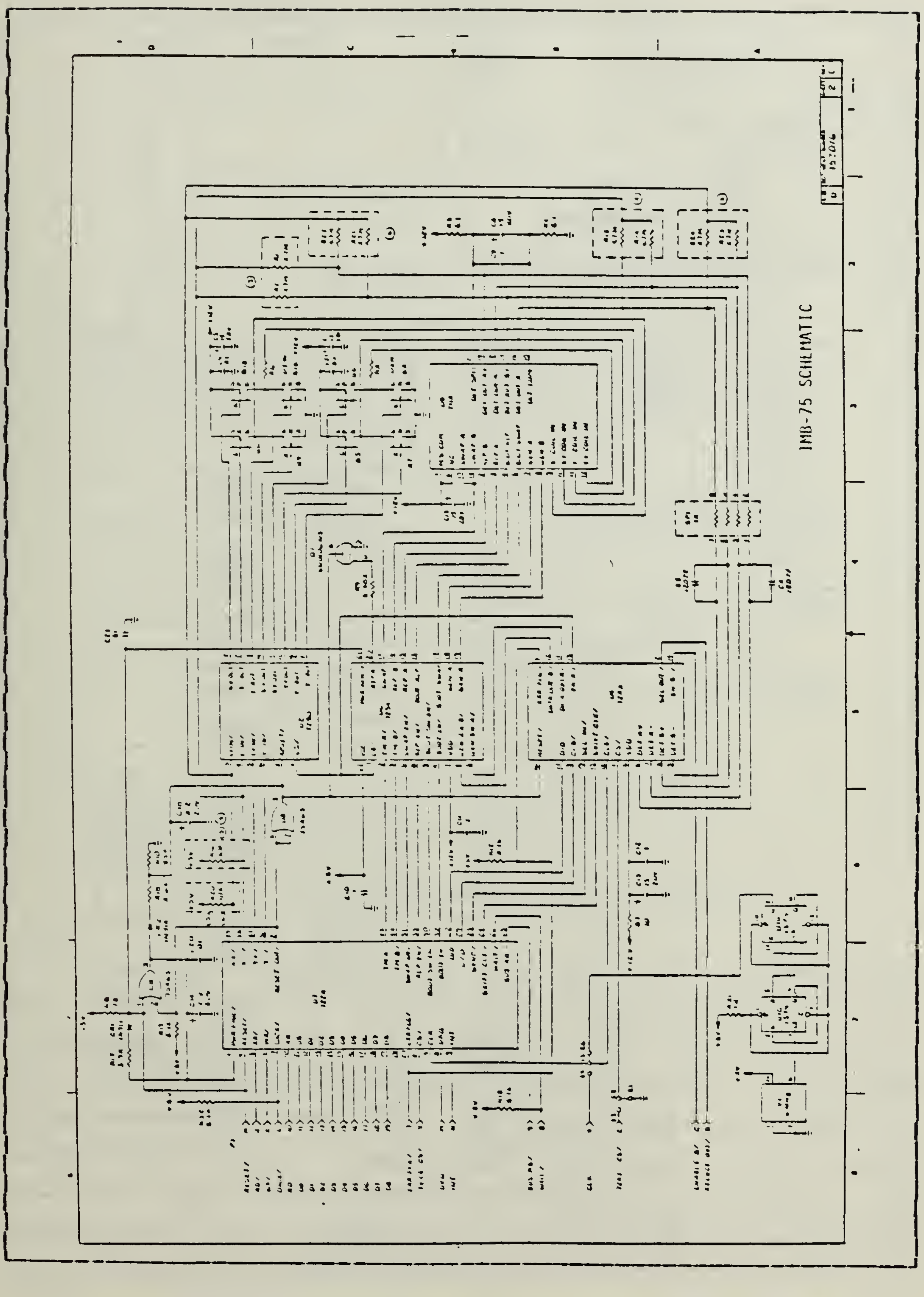


Figure B.10 Four-Megabit System Circuit Diagram.

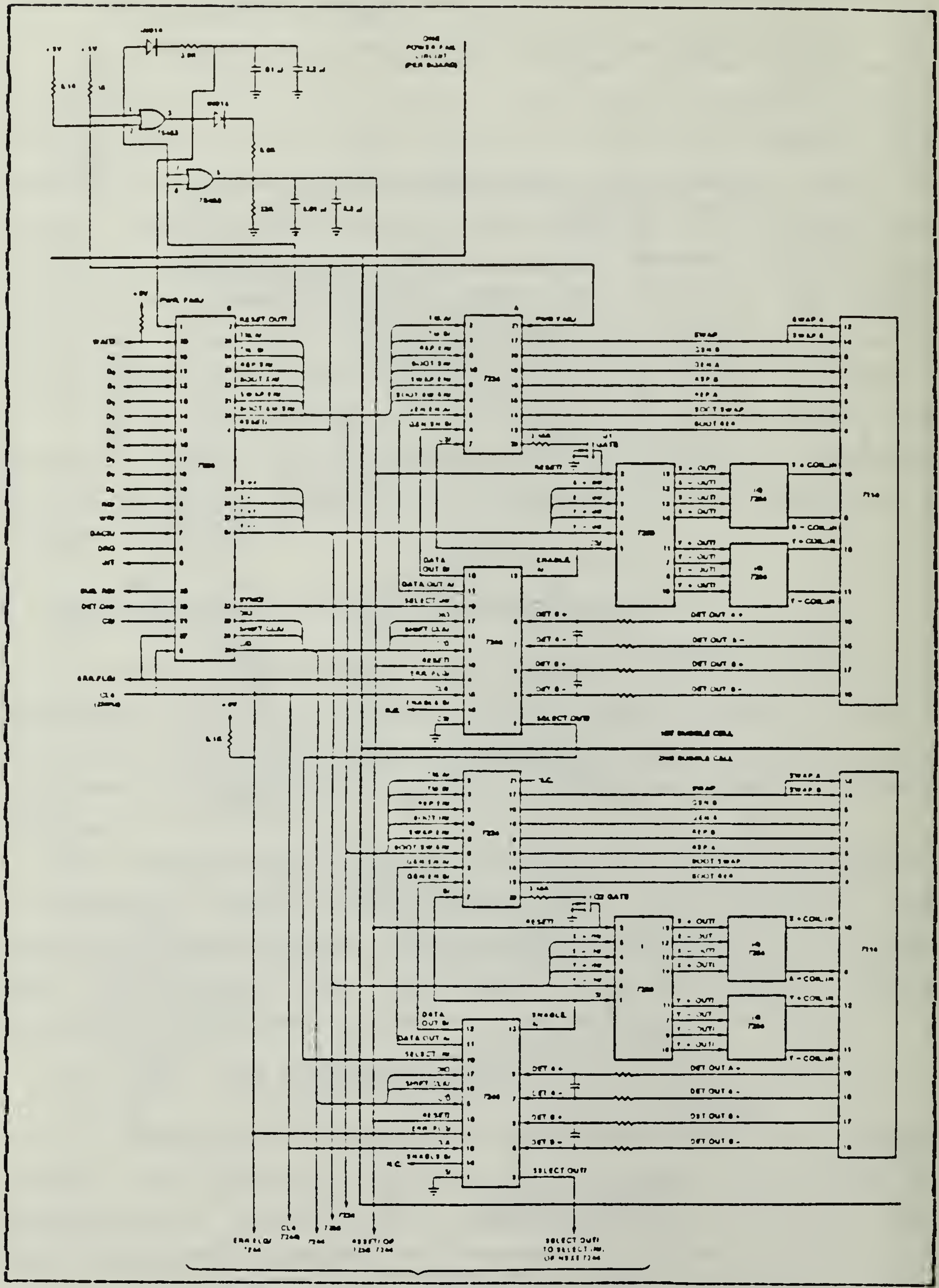


Figure B.11   Memory System Expansion.

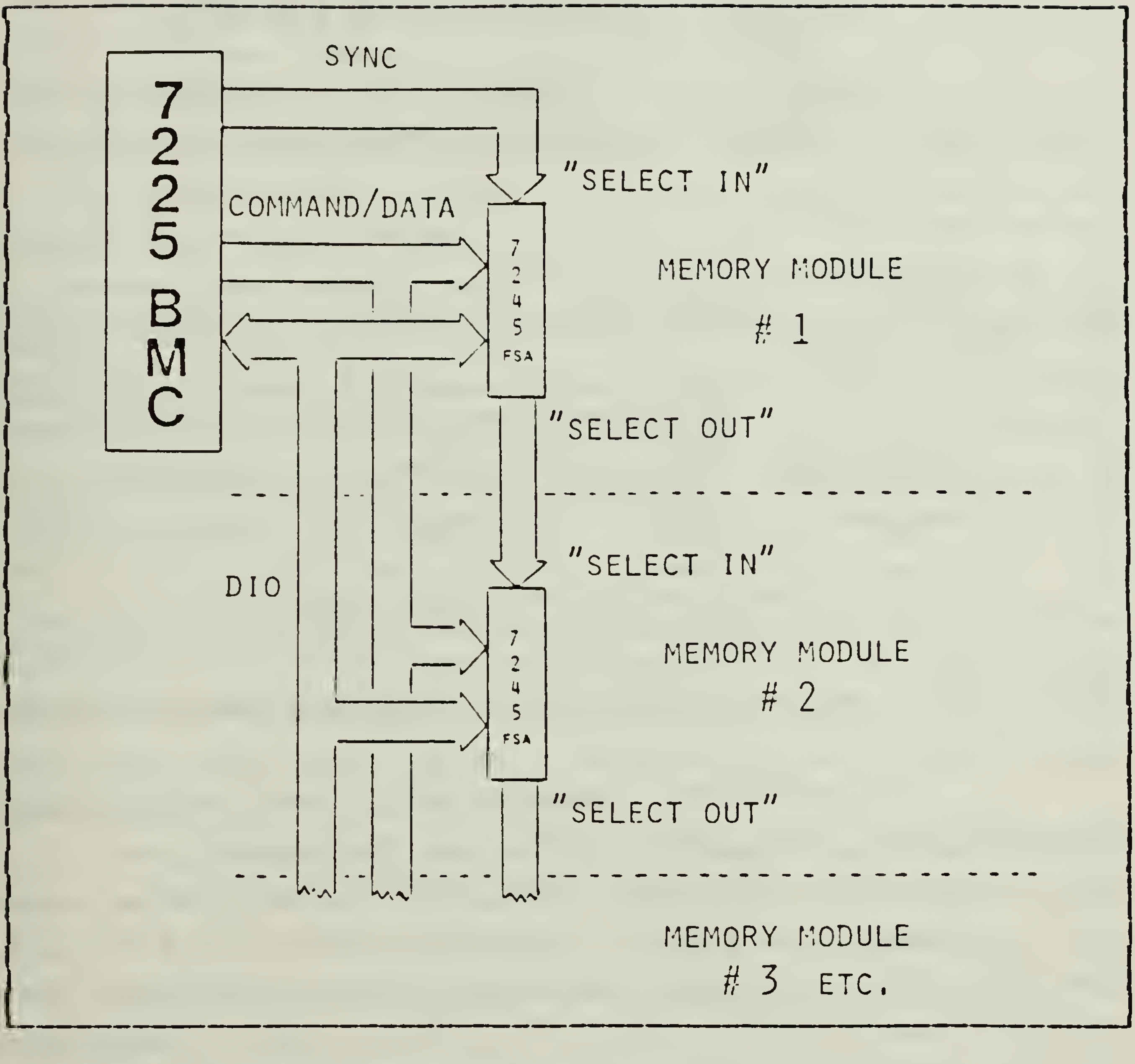


Figure B.12 BMC - FSA Communications.

In order to share the same DIO serial communication line between the BMC and the FSAs, communication must be established with each FSA individually to avoid contention over the single line. This is done by passing an enabling signal from FSA to FSA via the chip "select in" and chip "select out" lines. Commands and data sent over the single DIO line are differentiated by the signal level on the command/data line shared commonly by all FSAs in the system.

a. Establishing communication and commands

Figure B.13 is used to explain multiple module accessing and command by the bubble memory controller.

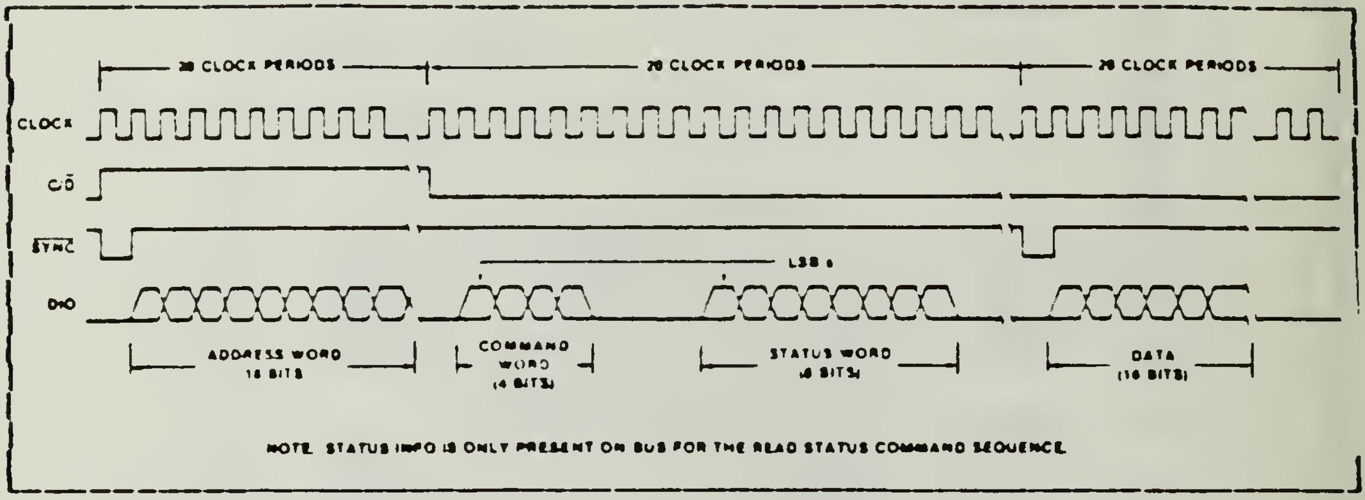


Figure B.13 **Access and Command of Multiple Memory Modules.**

To establish communication, the BMC indicates "command" by a high level signal on the command/data (C/D) line, pulses the first FSA "select-in" line (SYNC as shown in the figure), and sends a 16-bit address word serially over the DIO. Each pair of address bits corresponds to a separate memory module FSA; the first two bits correspond to the first FSA in sequence, the next two bits to the second FSA, etc. The maximum number of FSAs and memory modules that may be addressed by the bubble memory controller therefore is eight.

The first FSA delays the SYNC signal by two BMC clock cycles and then repeats the pulse on its own chip "select out" line which is connected to the following FSA chip "select in" line. During these two clock cycles, the FSA is enabled and looks for two high level pulses on the DIO line. If the pulses are received, communication with the module is requested and the FSA stands by to receive a four-bit command when the C/D line is lowered indicating data. If two "ones" are not received then that module is not involved in the up-coming operation and remains on standby. Elements within the standby module are not enabled by the FSA and ignore timing and other signals from the BMC on the other common lines.

The SYNC pulse is delayed two clock cycles within each FSA before the signal is passed on to the next sequential memory module. The C/D line is held high for 20 clock cycles no matter how many modules are in the system or how many modules are to be addressed. 20 additional clock cycles are allocated after the C/D line is lowered for the BMC to send out the four-bit command code and, if the command is to check the FSA status (only one module can be addressed at a time for this operation), to receive the eight-bit status word from the addressed FSA. It is after this point that data may be transferred between the BMC and FSAs in the method described next.

Note that the four-bit command codes sent by the BMC over the DIO are read simultaneously by all enabled FSAs when the C/D line is lowered. This indicates that all enabled modules perform the same functions when operating in parallel.

(1) Multiple Module Data Transfers. Figure B.14 depicts the timing involved when the received command from the BMC calls for data transfers. The SYNC pulse on the first FSA chip "select in" line enables it to access the DIO line. Since this signal is delayed two BMC clock cycles, only two bits of data are transferred with a single module each BMC SYNC pulse. The SYNC pulse is daisy-chained down the line of FSAs and the BMC correlates bits in sequence on the DIO line to the enabled FSAs. A new SYNC pulse is sent out by the BMC every 20 clock cycles until at least one "page" of data has been transferred between the

BMC and each FSA involved in the operation. This set timing scheme establishes the data transfer rates and required page sizes associated with different memory module accessing configurations.

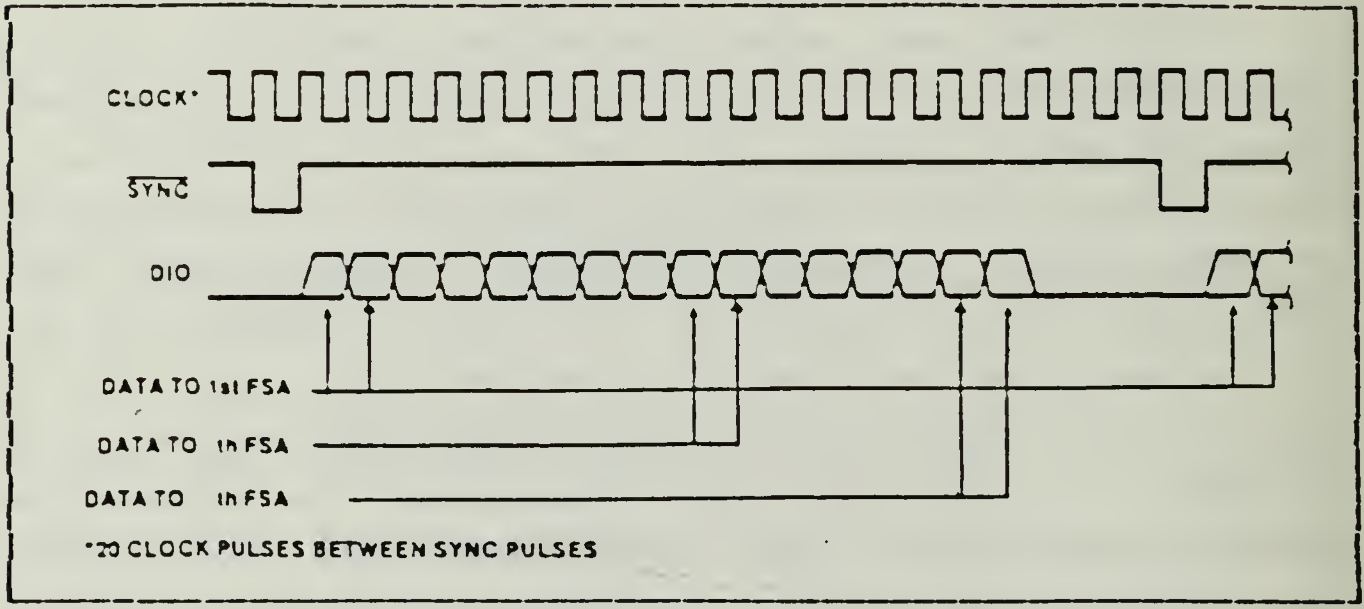


Figure B.14 Multiple Module Data Transfers.

H. OPERATING LIMITATIONS AND REQUIREMENTS

This section will outline the operating limitations of the bubble memory system and describe some of the system requirements including recommended support circuits.

1. Operating Limitations

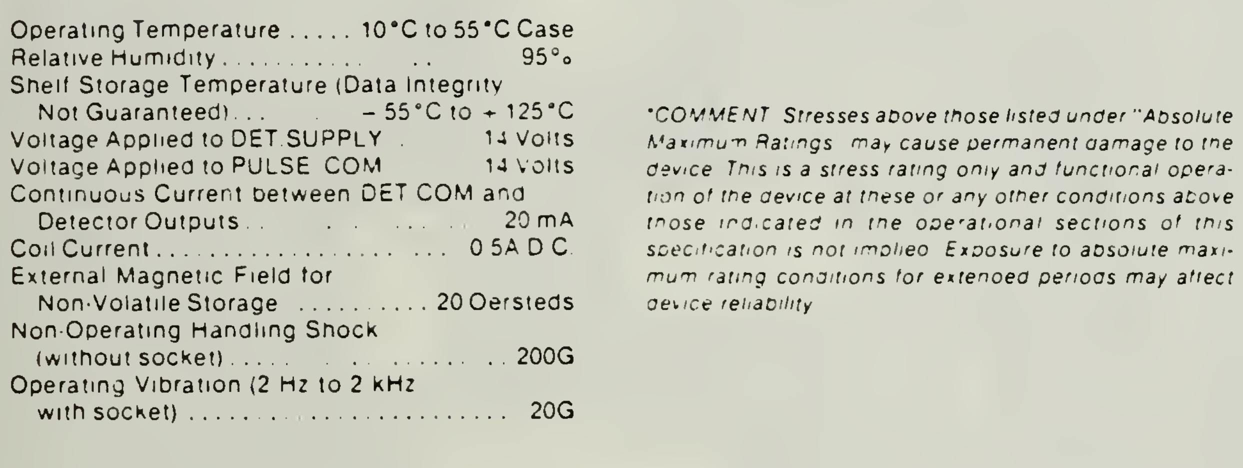
Table 18 lists some of the operating limitations of the 7114 magnetic bubble memory chip.

2. Voltage Regulator Circuitry

Figure B.15 depicts a voltage regulation circuit used by Intel on the BPK prototype kit. Intel recommends that multi-module configurations, such as described in

TABLE 18

7114 Absolute Maximum Ratings



Operating Temperature	10°C to 55°C Case
Relative Humidity	95%
Shelf Storage Temperature (Data Integrity Not Guaranteed)	−55°C to +125°C
Voltage Applied to DET SUPPLY	14 Volts
Voltage Applied to PULSE COM	14 Volts
Continuous Current between DET COM and Detector Outputs	20 mA
Coil Current	0.5A D.C.
External Magnetic Field for Non-Volatile Storage	20 Oersteds
Non-Operating Handling Shock (without socket)	200G
Operating Vibration (2 Hz to 2 kHz with socket)	20G

**COMMENT Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

Chapter 2, should include one voltage regulation circuit per memory board. The regulator circuit is intended to maintain the voltage supplies within tolerated limits which are +5V DC (+/- 5%) and +12V DC (+/- 1%).

3. Powerfail Circuit

Figure B.11 depicted a powerfail circuit associated with the bubble memory system. The circuit is designed to detect if either of the required power sources fall beneath the low-end margins for operation (-5% on the 5V supply and -1% on the 12V supply). The circuit assists the 7234 CPG which provides the powerfail signal to the bubble memory controller to shut down the system in a manner which preserves data integrity.

The circuit also contains storage elements to maintain adequate power for proper system shut-down, and a powerfail signal delay circuit to prevent powerfail indications during system power-up.

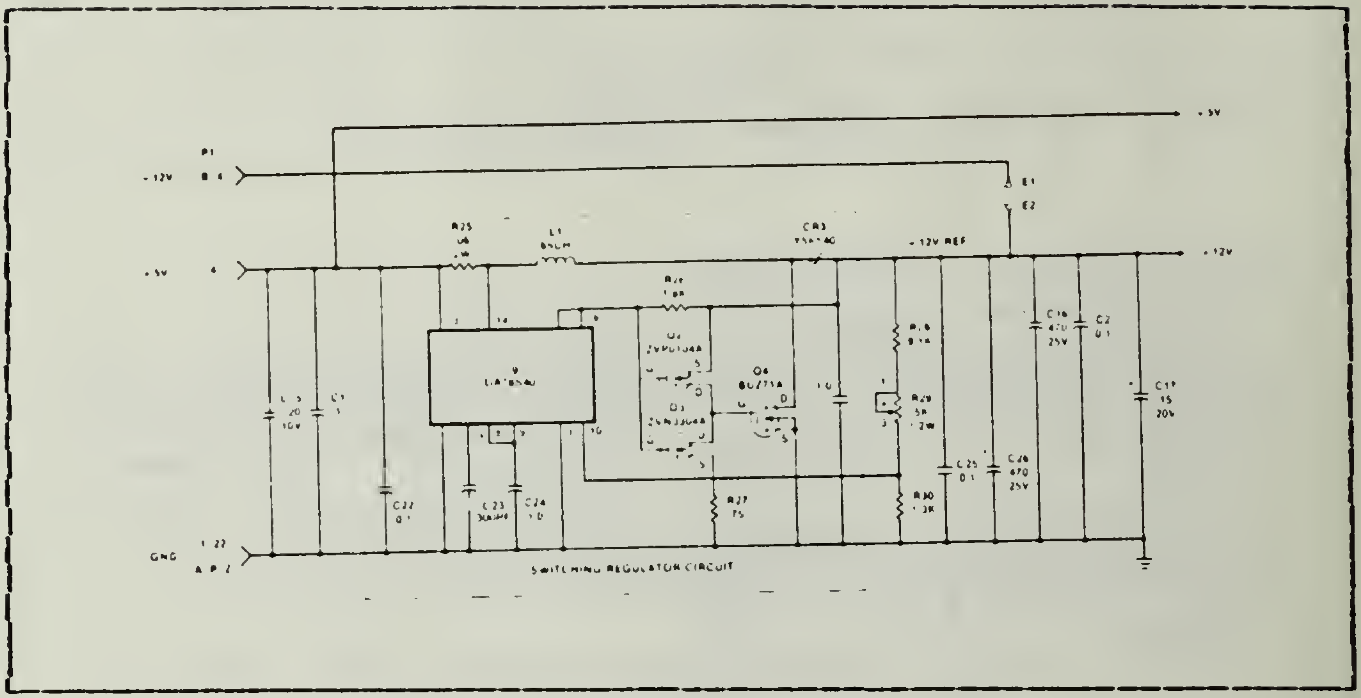


Figure B.15 Voltage Regulator Circuit.

I. THE BPK 5V75A PROTOTYPE KIT

Figure B.16 depicts the BPK 5V75A four-megabit magnetic bubble memory prototype kit presently available from Intel. The kit is basically a single memory module with a dedicated 7224 bubble memory controller chip and necessary support circuits. The major components and circuits are annotated on the figure. Of particular interest are the voltage regulator and powerfail circuits, dual 7245 formatter/sense amplifiers, and external EPROM. The dual FSAs and EPROM are part of the External Added Redundancy Scheme (EARS) modification Intel has incorporated to increase the production yield of useable devices.

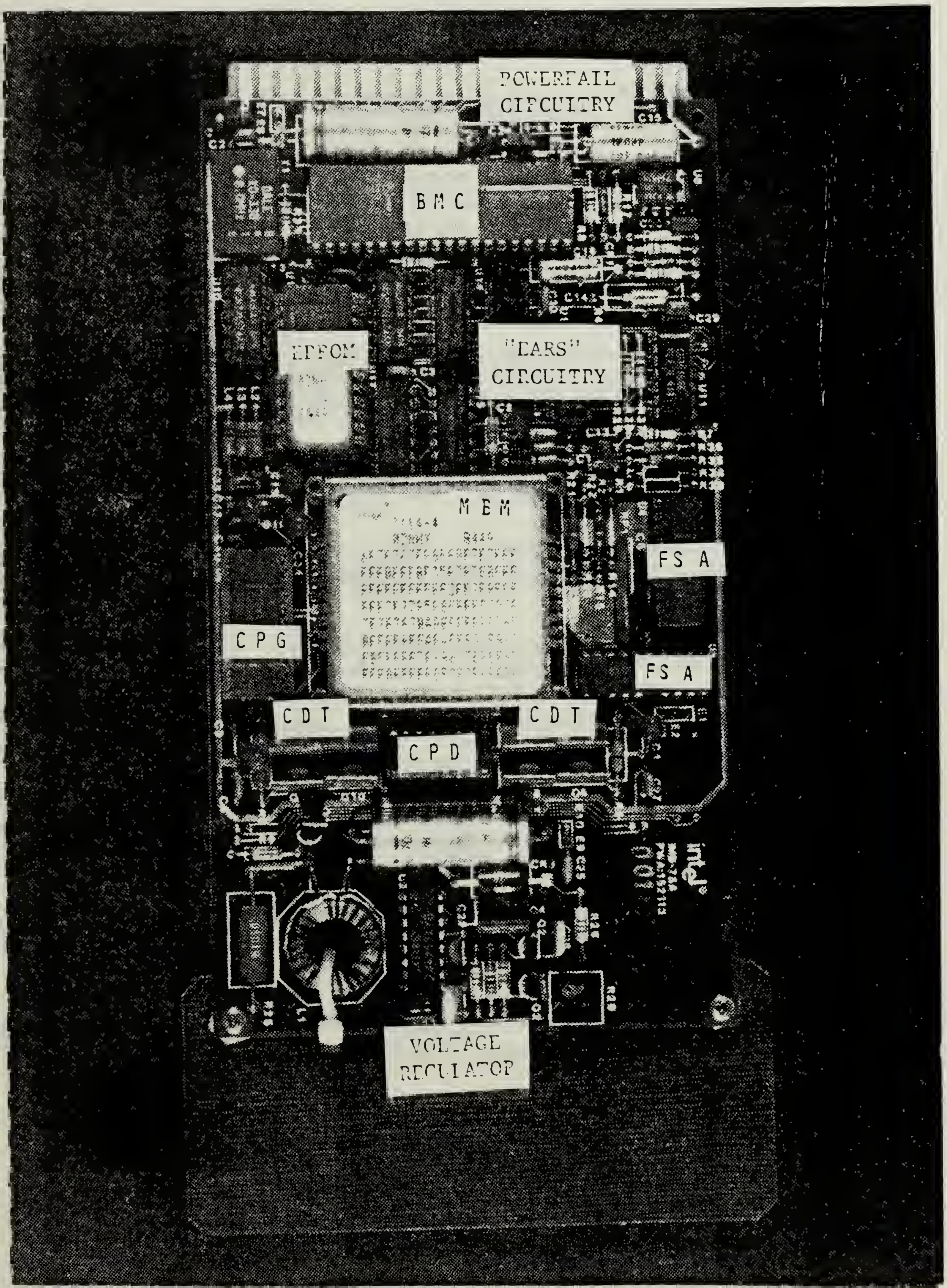


Figure B.16 BPK 5V75A Prototype Kit.

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